

# Perancangan Elektronika Berbantuan Komputer

## PENDAHULUAN

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# Electronics Modern Design

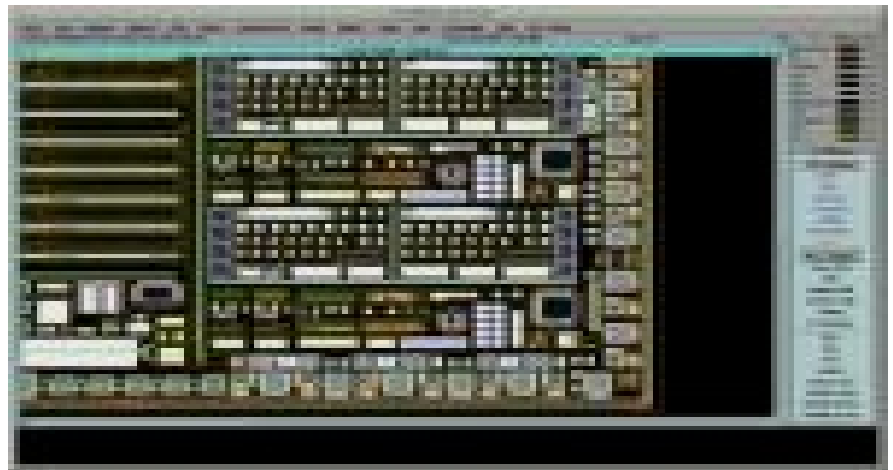
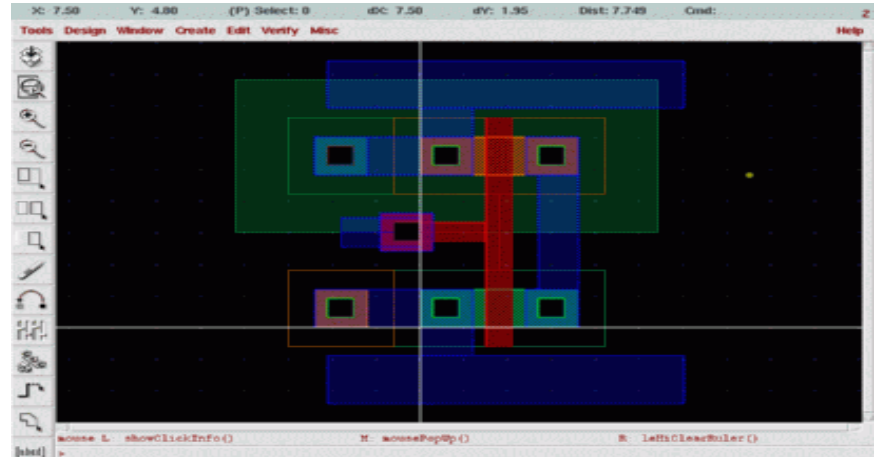
- Using Software tools why ?
  - Fast design
  - Circuits complexity
  - Based on VLSI
  - Small Size
  - ETC

# Issues

- Software Tools Design
- CHIP Fabrication
- Cost
- How to design the transistor circuits into the CHIP

# Software Tools Design

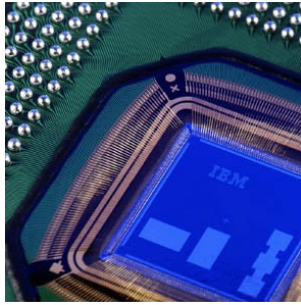
- LASI, MAGIC, DREAM
- MAX, MyCAD LAYED
- Cadence
- Synopsis
  
- Mentor Graphics



# CHIP Fabrication

- CMP-TIMA, France
- TSMC, Taiwan
- NEC, Japan
- Mosis, USA
- Mimos, Malaysia ?
- Etc





# Cost

- Austria Micro Systems
  - 0.6 CMOS CUP 390 Euro/mm<sup>2</sup>
  - 0.35 CMOS C35B4C3 650 Euro/mm<sup>2</sup>
- STMicroelectronics
  - 0.18 CMOS HCMOS8D 990 Euro/mm<sup>2</sup>
  - 0.12 CMOS HCMOS9GP 2500 Euro/mm<sup>2</sup>
  - 90 nm CMOS CMOS090 5000 Euro/mm<sup>2</sup>

# How to design ...

## Case : Pipeline ADC design

- First Step :
  - Architecture Circuit Design

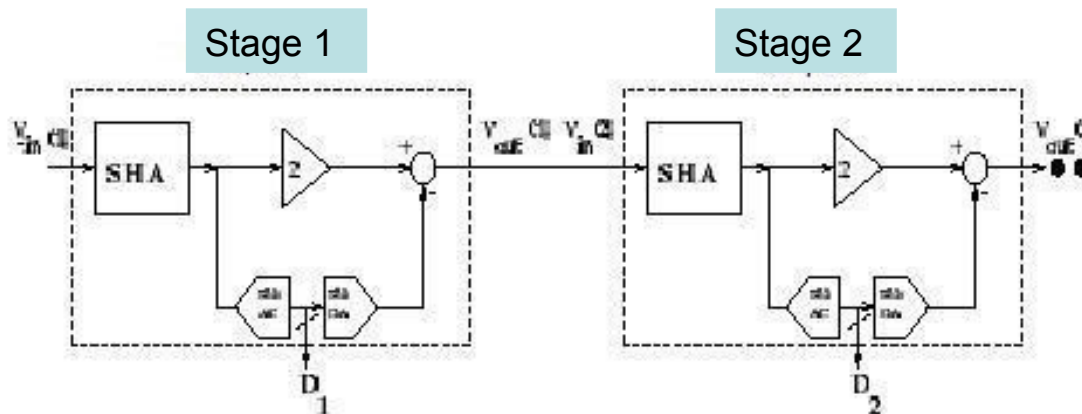
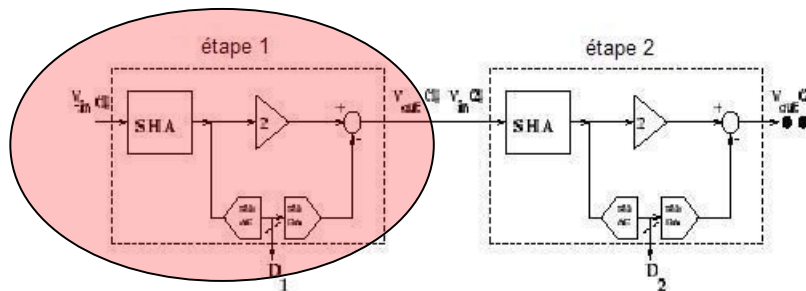


Diagram Block of One bit per stage

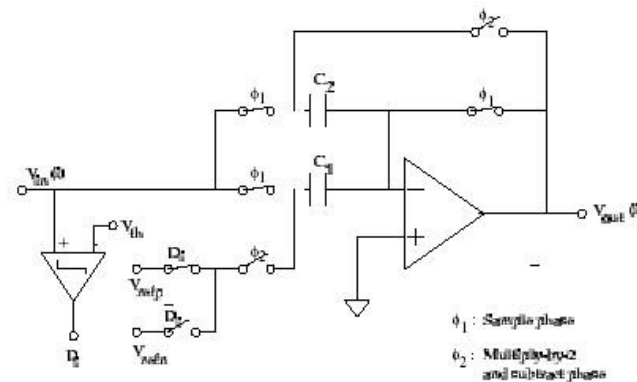
# How to design ...

## Case : Pipeline ADC design

- First Step :
  - Architecture Circuit Design



Implemented by  
Switched Capacitor



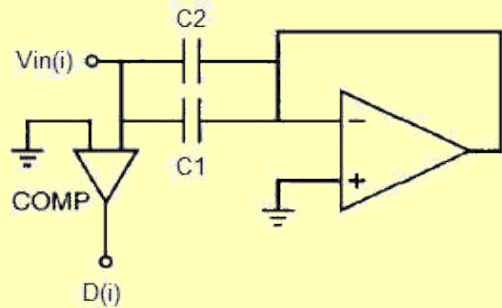


# How to design ...

## Case : Pipeline ADC design

- Each stage operates in two phase :
  - Sampling phase
  - Multiplying Phase

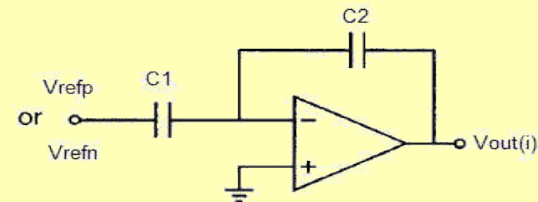
### Sampling Phase



Sampling phase

1.  $V_{in}$  is stored in capacitors
2. Comparator produces a digital output  $D$ 
  - ✓  $D = 1$  if  $V_{in} > (V_{refp} - V_{refn}) / 2$
  - ✓  $D = 0$  if  $V_{in} < (V_{refp} - V_{refn}) / 2$

### Multiplying Phase



Multiplying phase

1. If  $D = 1$ 
  - ✓ Capacitor  $C1$  connect to  $V_{refp}$
  - ✓  $V_{out} = 2 * V_{in} - V_{refp}$
2. If  $D = 0$ 
  - ✓ Capacitor  $C1$  connect to  $V_{refn}$
  - ✓  $V_{out} = 2 * V_{in} - V_{refn}$

# How to design ...

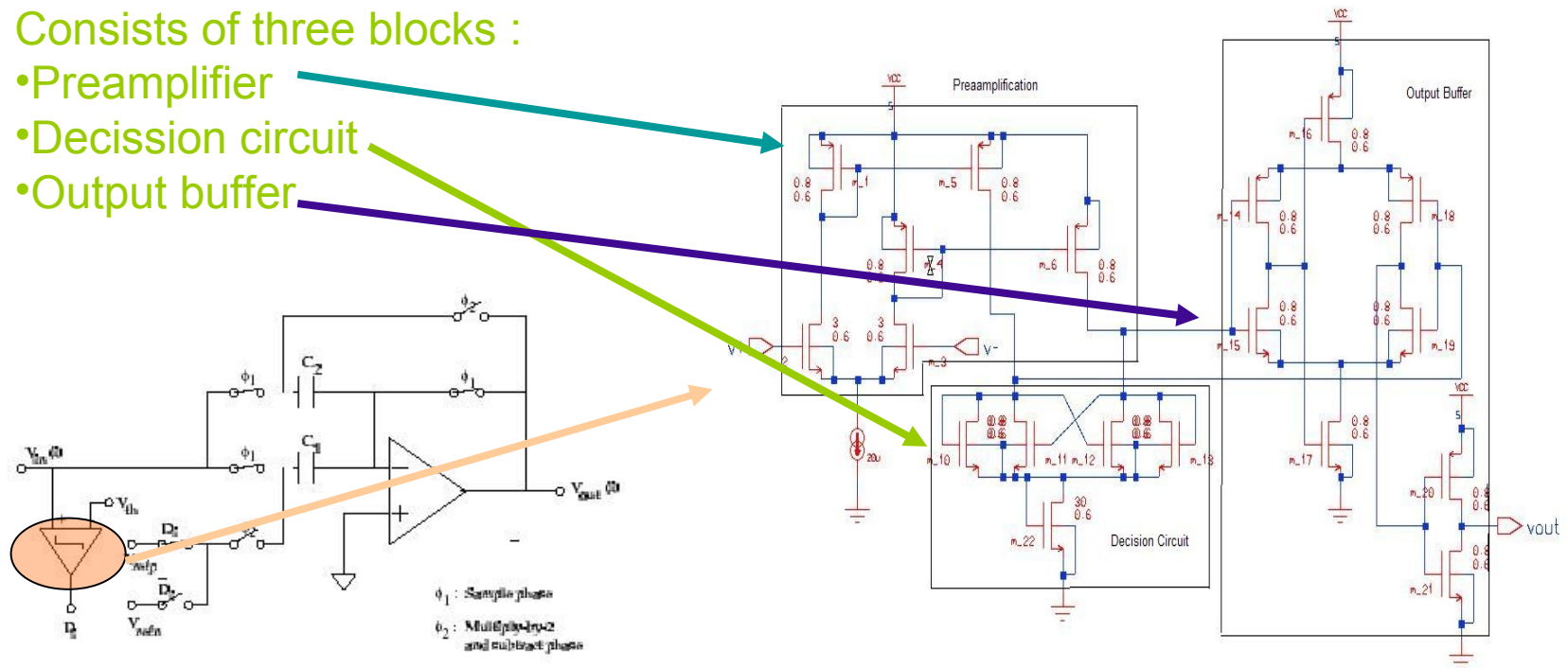
## Case : Pipeline ADC design

- First Step :
  - Architecture Circuit Design

### Comparator

Consists of three blocks :

- Preamplifier
- Decision circuit
- Output buffer



# How to design ...

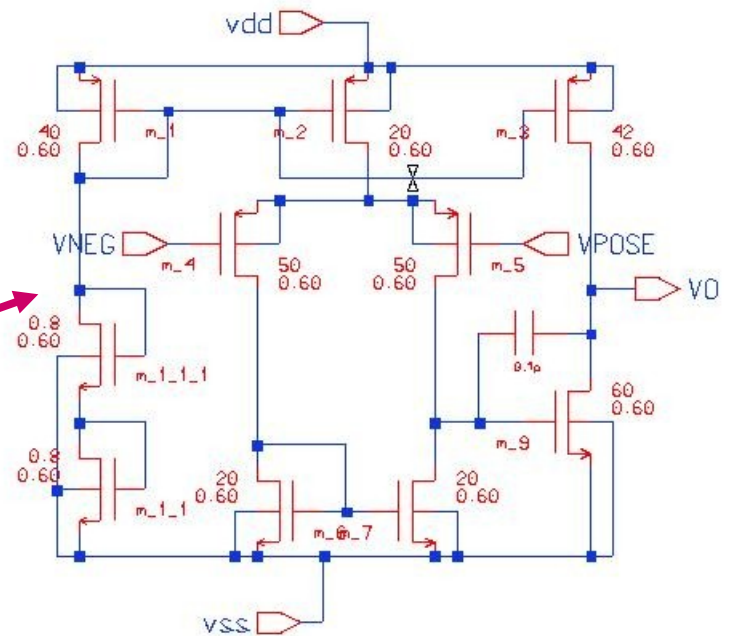
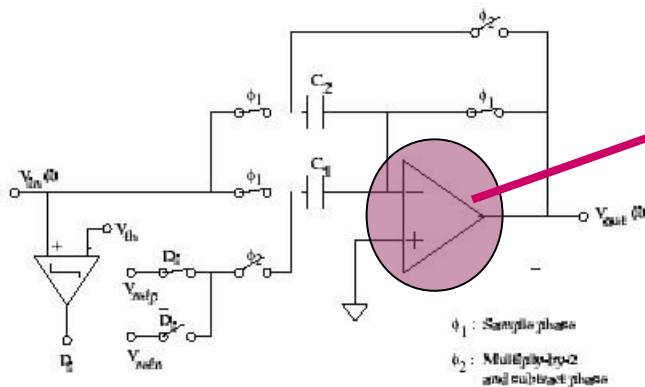
## Case : Pipeline ADC design

• First Step :

• Architecture Circuit Design

### Operational Amplifier

➤  $V_{dd} = 5\text{ V}$  and  $V_{ss} = -5\text{ V}$



# How to design ...

## Case : Pipeline ADC design

- Second Step :
  - Done Simulation
    - Result of simulation of Operational Amplifier

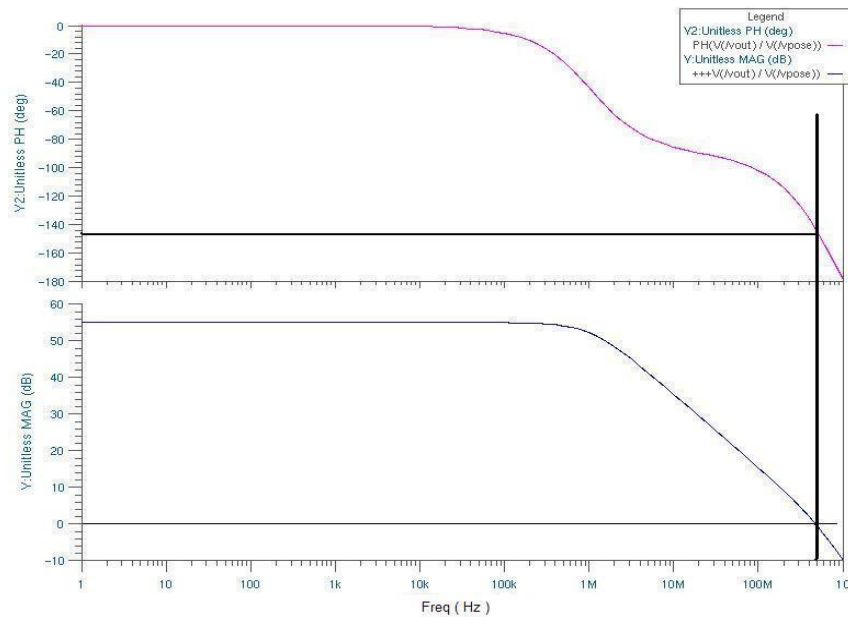


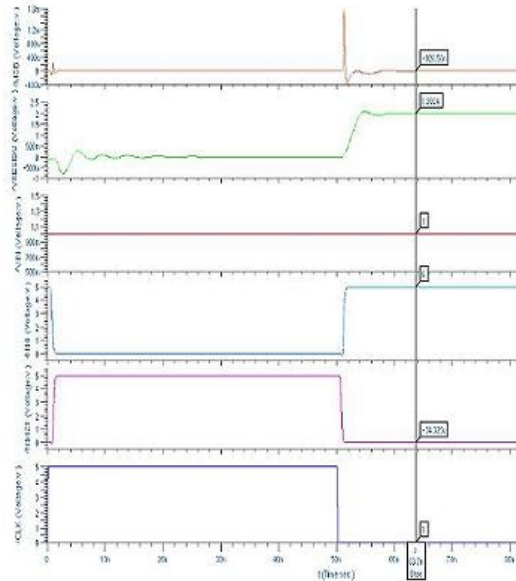
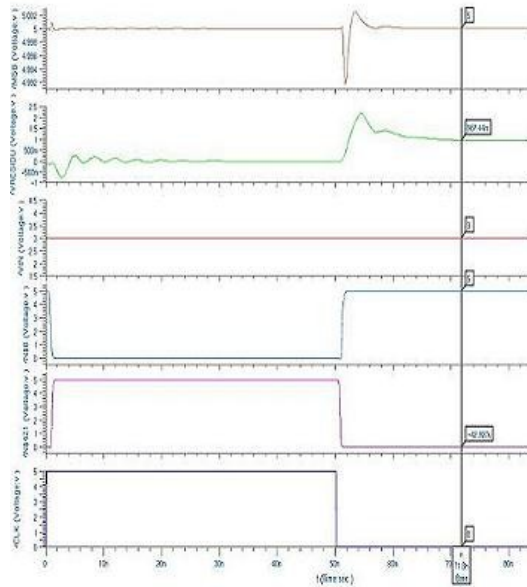
Table 1: OP-Amp Performance

Gain	PM	Gain Bandwidth	Power
55	-145°	800 MHz	10.825 mW

# How to design ...

## Case : Pipeline ADC design

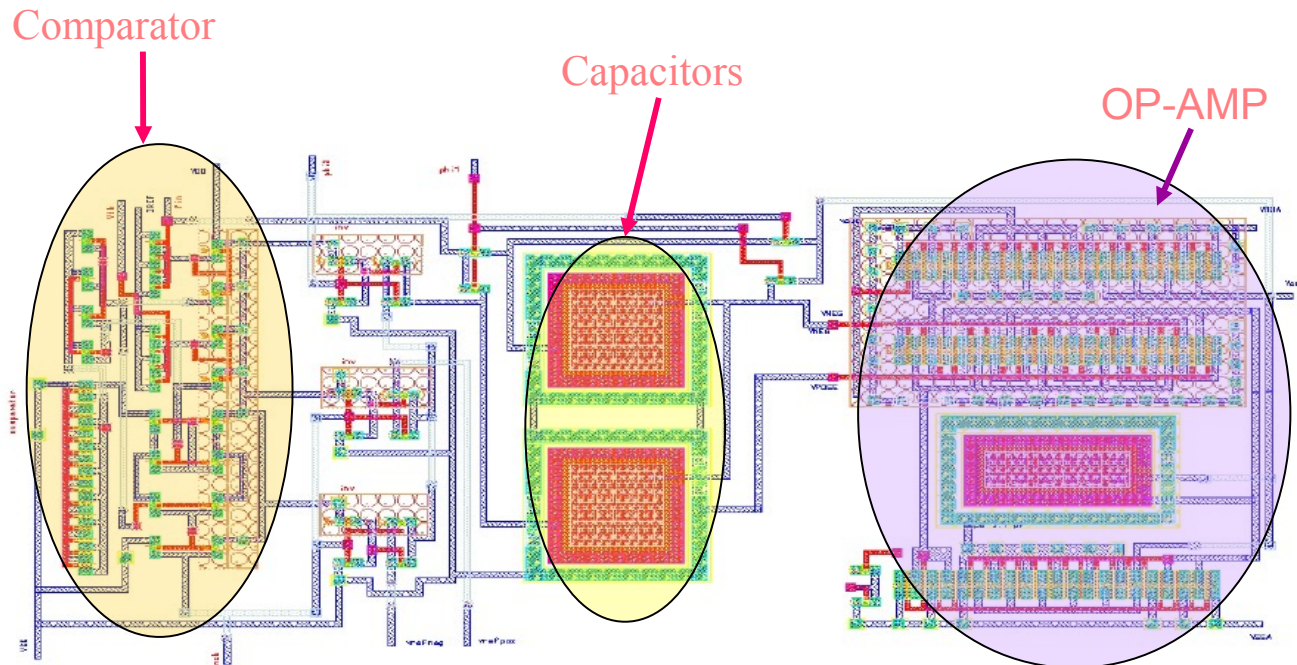
- Second Step :
  - Done Simulation
    - Result of simulation of one bit per stage pipeline



# How to design ...

## Case : Pipeline ADC design

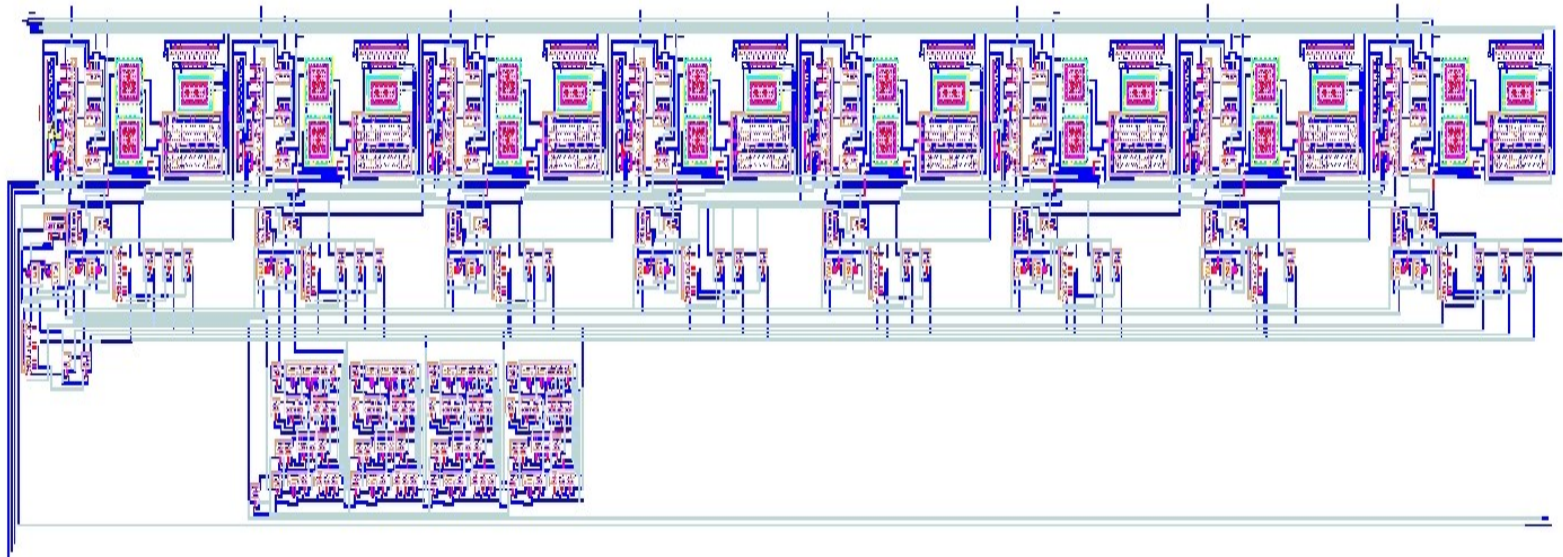
- More Step :
  - Made Layouts
    - One stage A/D converter layout



# How to design ...

## Case : Pipeline ADC design

- More Step :
  - Layouts Design
    - 8 bits A/D converter layout



# How to design ...

## Case : Pipeline ADC design

- More Step :
  - Layouts Design
    - 8 bits ADC layout of CHIP photograph

