# Perancangan Elektronika Berbantuan Komputer

# PENDAHULUAN

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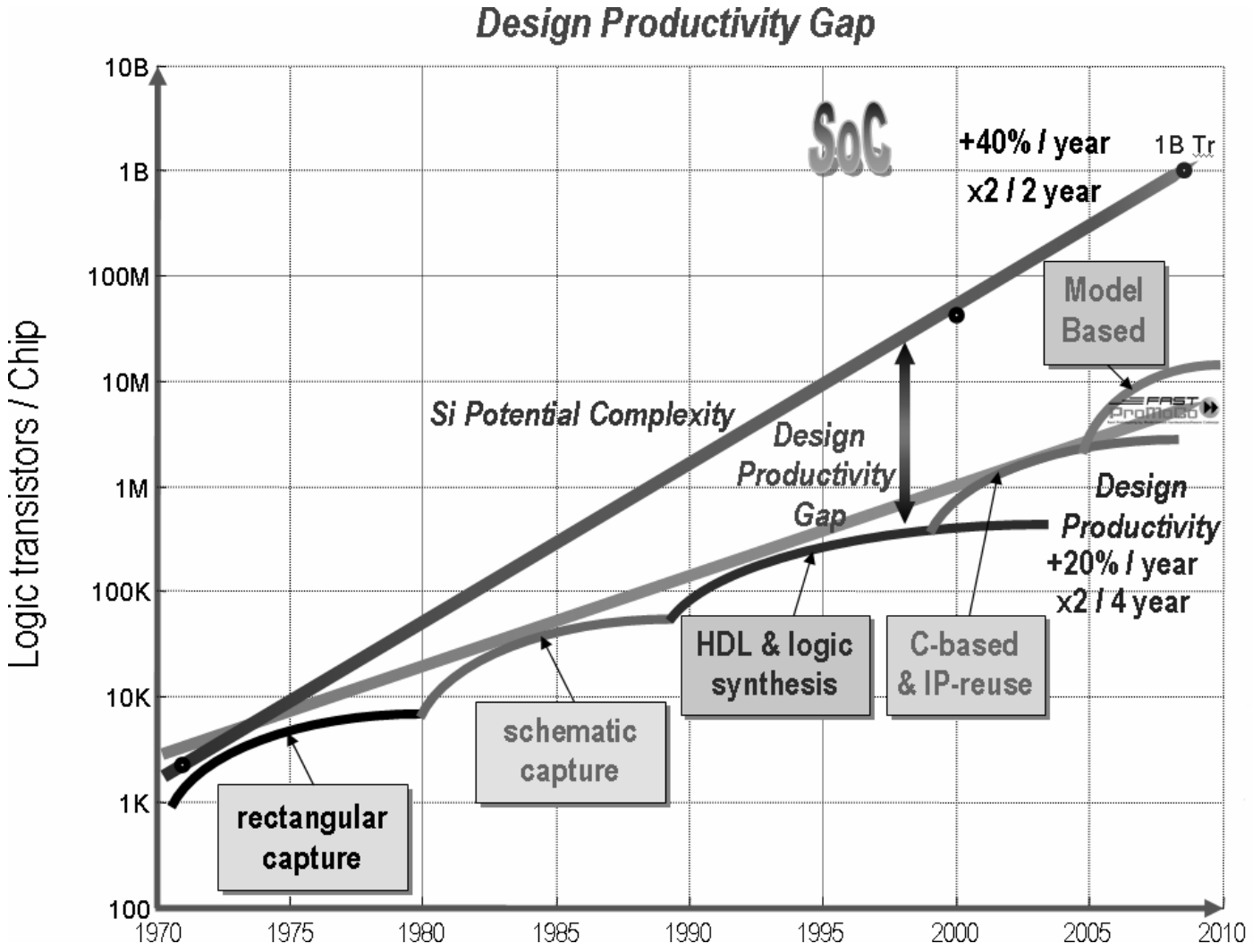
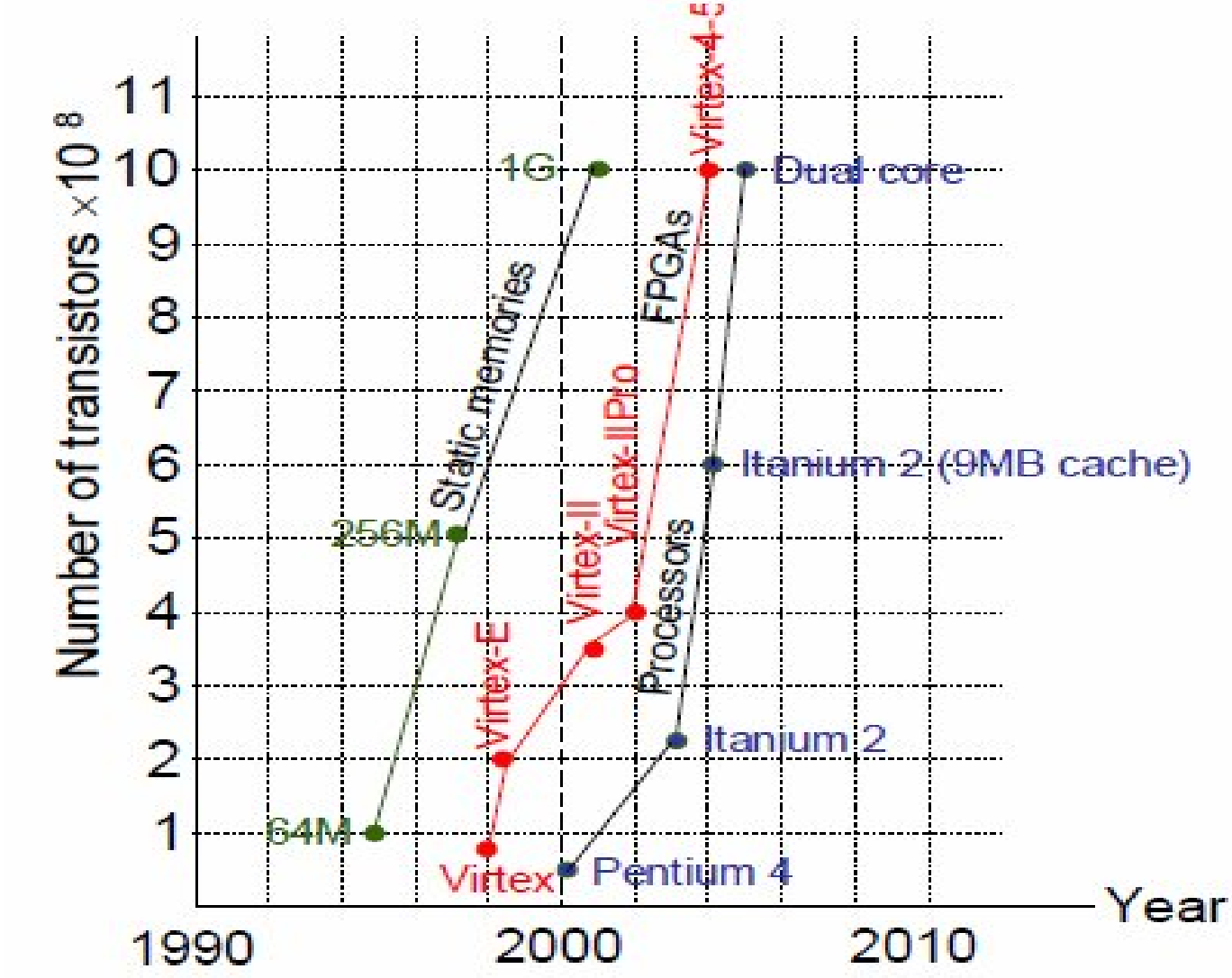



Moore's law and resulting Design Productivity Gap

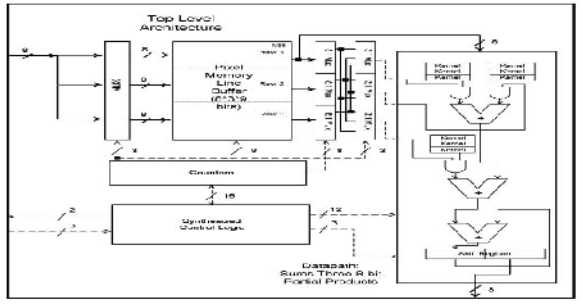



**g. 1. Relevancy of the Moore's law to different microelectronics products**

# Mengapa terpadu ?

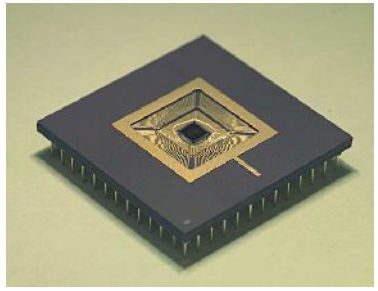
kelebihan :

- Tempat ringkas
- Hemat energi
- modular
- Lebih Aman



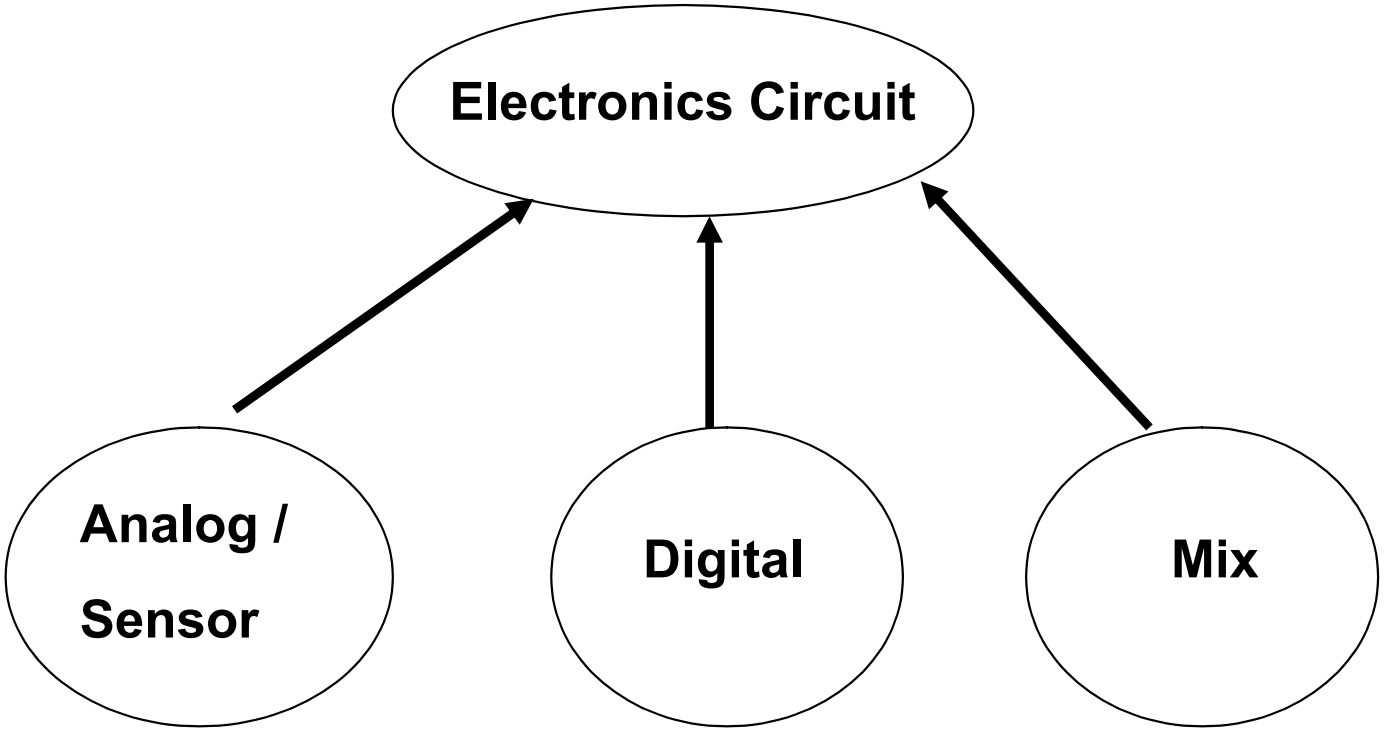
Système électronique

Circuit électronique



Composant: Circuit intégré

# Metodologi Desain



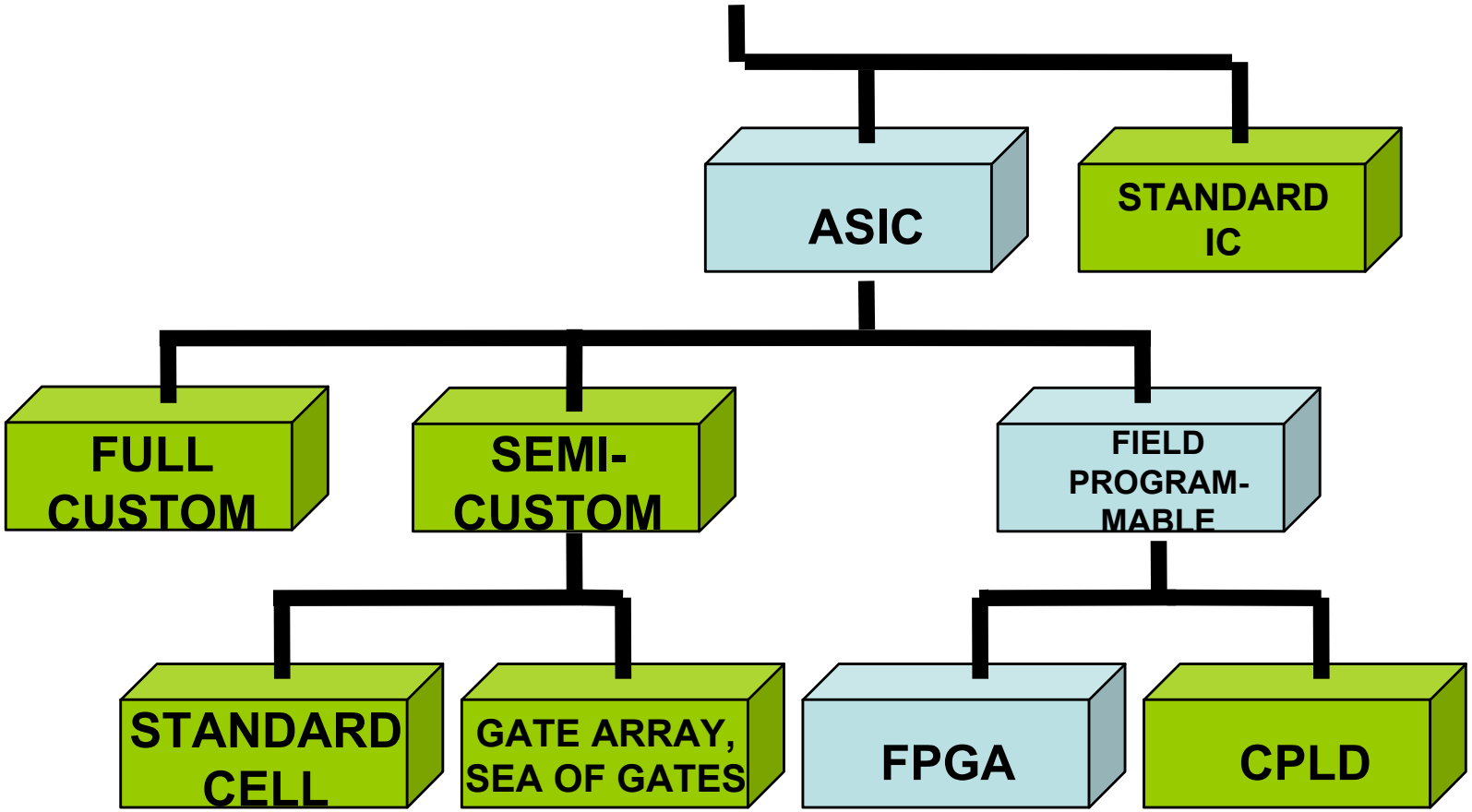
# Bagaimana Mendesain ?

- Langsung di Protoboard ?
- Komponen yang digunakan ?
- Perlu adanya simulasi ?
- Bagaimana merealisasikan circuit ke bentuk Chips?
- Bagaimana untuk fabrikasi ?
- Perlu bantuan Software ?

# Electronics Modern Design

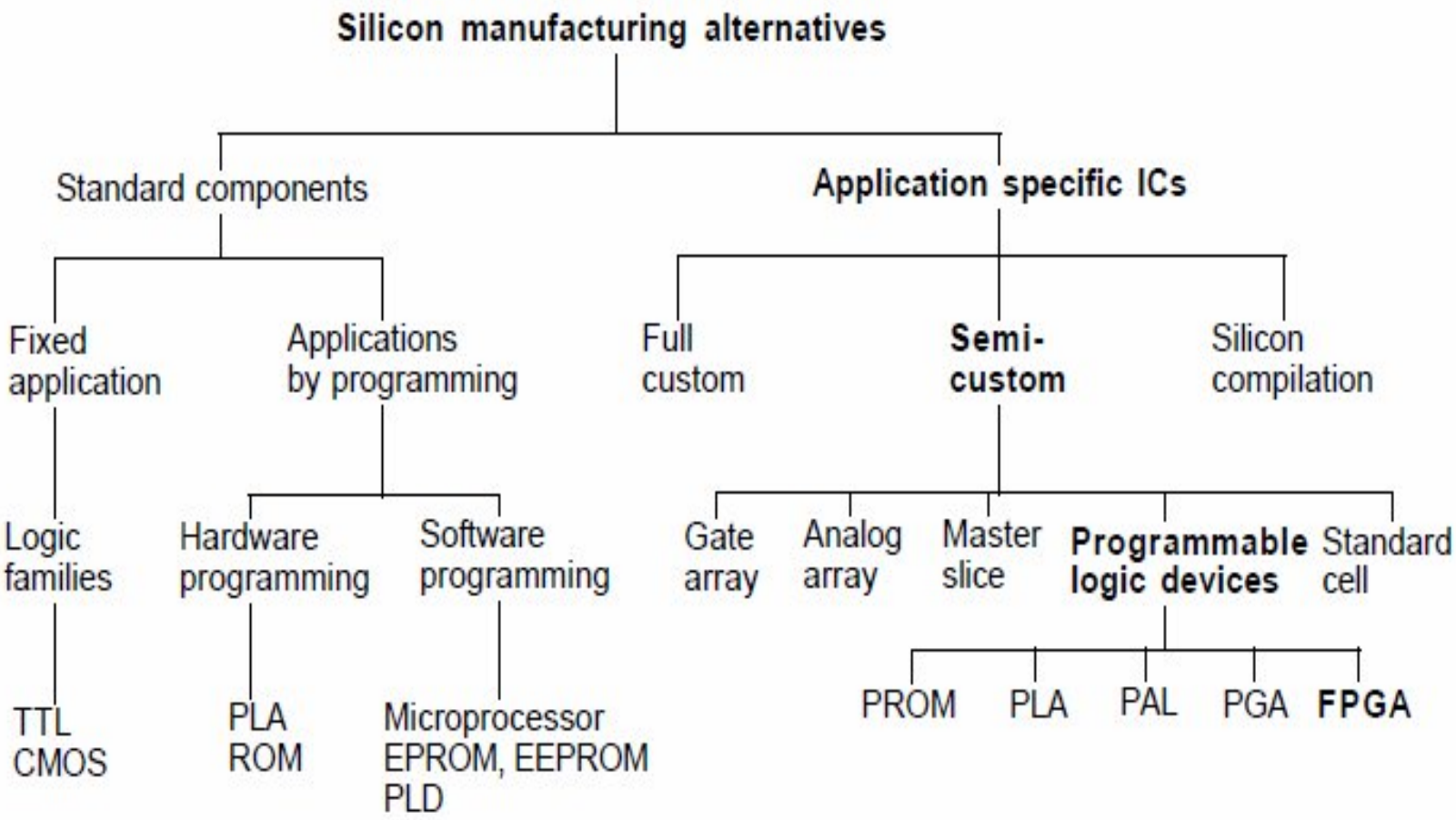
- Using Software tools  why ?
  - Fast design
  - Circuits complexity
  - Based on VLSI
  - Small Size
  - ETC

# Proses Desain



# Silicon Manufacturing Alternatives

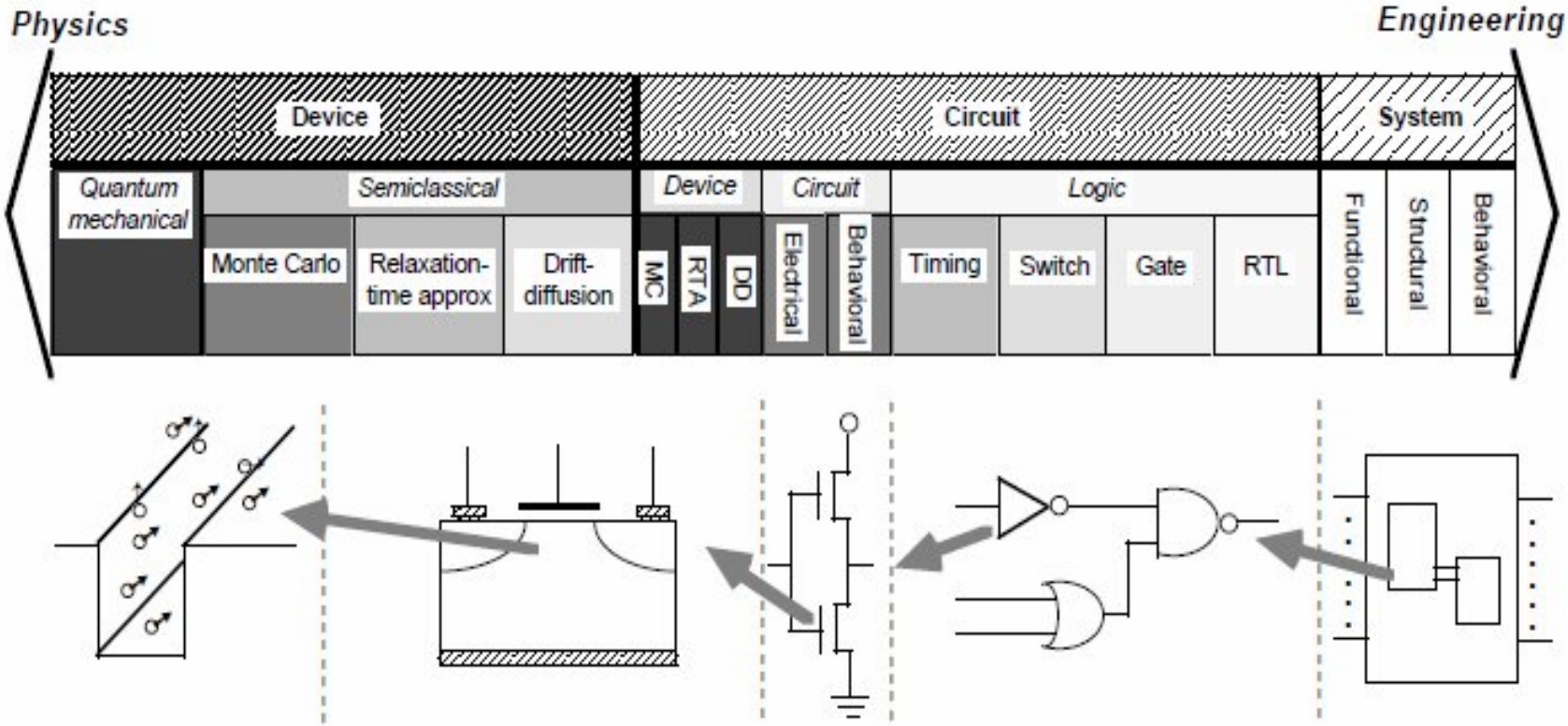




# Spectrum of Approaches to Electronic Systems



## The "Big Picture"



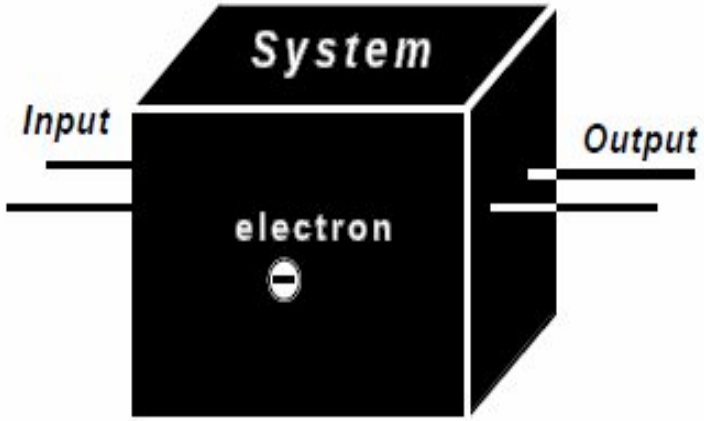
# Motivation



- Question: *Why so many levels of abstraction?*

***Electronic System:***

A "black box" which performs a certain function based on the laws of physics of the "electrons"

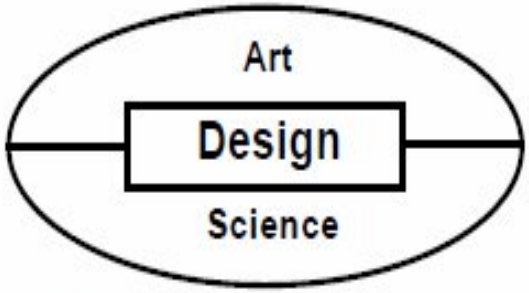



- Answer:

> "Everything should be made as simple as possible, but not any simpler."
>
> — *Albert Einstein*

# The Art–Science Dichotomy of Design Activities



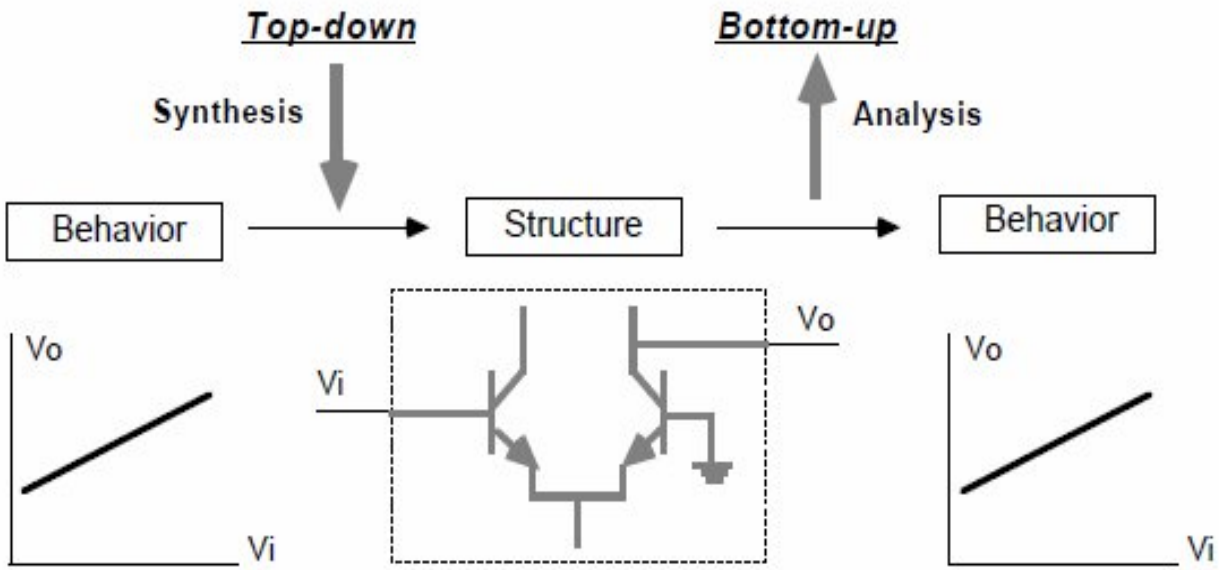



| | *Perspective* | | *Tools* | |
|---|---|---|---|---|
| Art | Innovation | Human | ? | – Creativity |
| | Decision making | | KBES | – Productivity |
| Science | Transformation | Machine | CAD | – Productivity |

- ***Decision-making perspective***: a creative process involving individual talent, intuition, experience, etc.
- ***Transformation perspective***: a process of successive transformations of specifications from one domain (abstraction level) to another

# Two Fundamental Approaches of a Design






- **Analysis**
  - Application of well-known principles to predict the behavior of a system
- **Synthesis**
  - Selection of a solution from a number of alternatives based on a set of criteria
  - An ensemble of answers waiting for the right question

# Design Decisions



● *What* design decisions are to be made? ● *How* are they made?

- ❑ **Software/hardware trade-offs**
  - Affect the flexibility of the product (need to modify the design in the future)
- ❑ **Processing technology**
  - Figure of merit: gate delay, power consumption, noise immunity, logic capacity
- ❑ **Implementation style**
  - Standard cells, gate arrays, programmable logic devices, etc.
- ❑ **Choice of hardware algorithms**
  - Functional module designs in ROMs, RAMs, PLAs, etc., where regularity in the structure can be captured and exploited in a procedural fashion

***Note*** The first three decisions are largely influenced by marketing considerations such as design standards, compatibility requirements, expendability, product lifetime, and other economic factors, which can be determined before the actual design starts. In contrast, It may be necessary to delay the fourth decision due to uncertainties in meeting physical constraints such as chip area, power consumption, I/O bandwidth, or system partitioning.

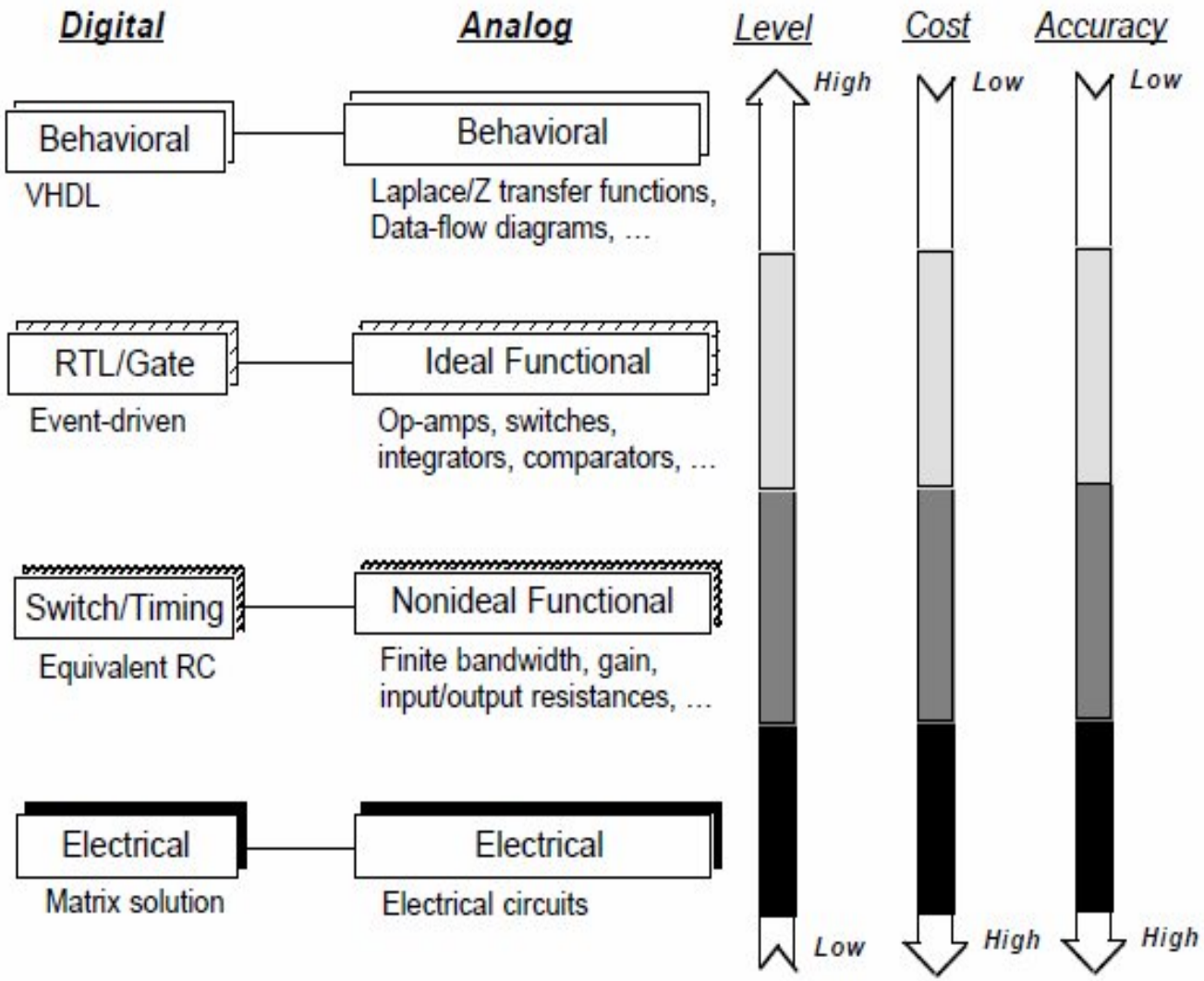
# Hierarchical Design Approach



- **To combat complexity — "divide-and-conquer"**
- **Hierarchical approach**
  - Partition various aspects of VLSI circuits into abstraction levels
  - Define the order among these levels
- **Methodology**
  - A particular ordered sequence of steps linking these abstraction levels
- **Implementation**
  - A set of CAE design tools
  - Efficient implementation depends on:
    - How well its underlying principles reflect the nature of VLSI circuitry
    - How well its external expressions supports the implementation efforts

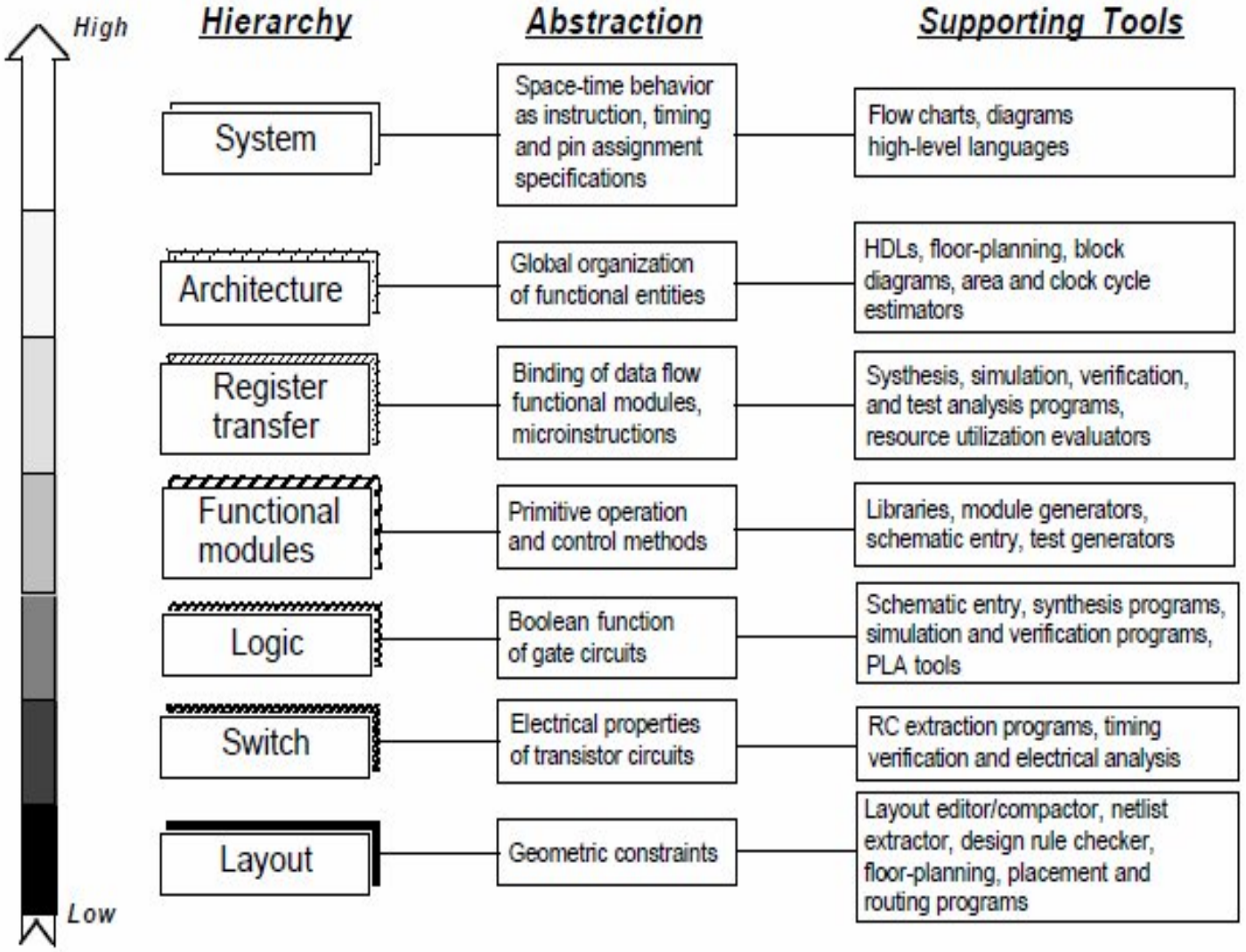
# Levels of Abstraction in Digital and Analog Design





# VLSI Design Hierarchy





# Introduction

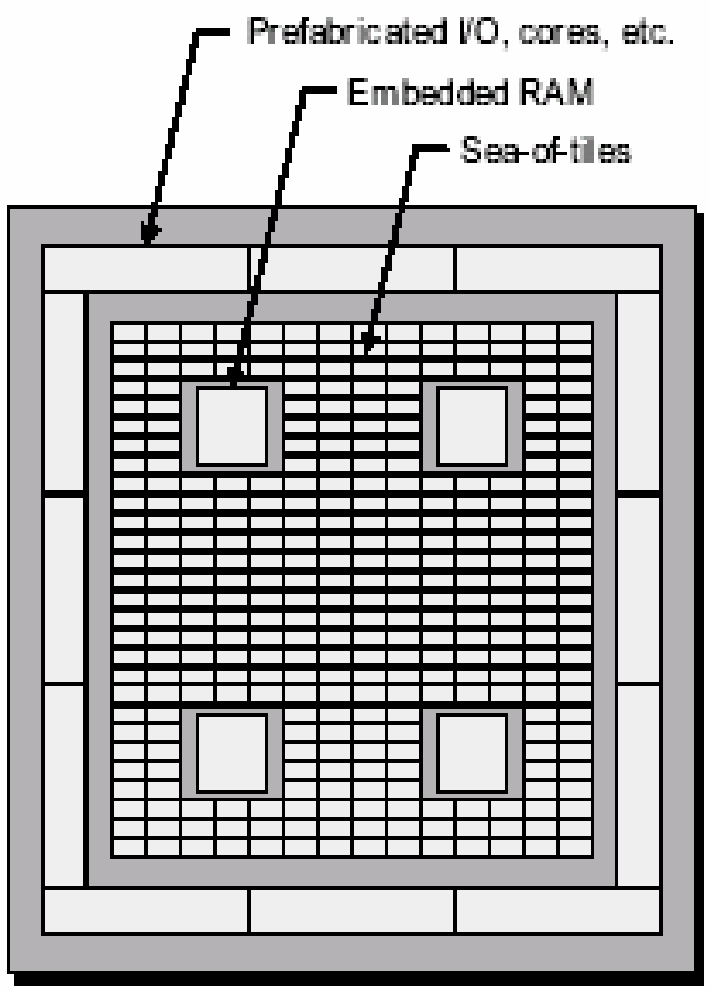
- A Structured ASIC falls between an FPGA and a Standard Cell-based ASIC
- Structured ASIC's are used mainly for mid-volume level designs
- The design task for structured ASIC's is to map the circuit into a fixed arrangement of known cells

# Properties

- Low NRE cost
  - Implementation engineering effort
  - Mask tooling charges
- High performance
- Low power consumption
- Less Complex
  - Fewer layers to fabricate
- Small marketing time
  - Pre-made cell blocks available for placing

# Architecture

- Two Main Levels
  - Structured Elements
    - Combinational and sequential function blocks
    - Can be a logical or storage element
  - Array of Structured Elements
    - Uniform or non-uniform array styles
    - A fixed arrangement of structured elements



# Main Implementation Steps

1. RTL Design
   - Register transfer level design
2. Logical synthesis
   - Maps RTL into structured elements
3. Design for Test insertion
   - Improves testability and fault coverage
4. Placement
   - Maps each structured element onto array elements
   - Places each element into a fixed arrangement

# Main Implementation Steps

5. Physical synthesis
   - Improves the timing of the layout
   - Optimizes the placement of each element
6. Clock synthesis
   - Distributes the clock network
   - Minimizes the clock skew and delay
7. Routing
   - Inserts the wiring between the elements

# Implementation Issues

- Logical synthesis, placement and routing all depend on the target structure element architecture and hence add more complexity to the design process.
- The completeness of the target structured ASIC library also affects what specifically can be implemented from the design.

# FPGA Vs. Standard Cell ASIC

- Easy to Design
- Short Development Time
- Low NRE Costs(dana riset, design dll)
- Design Size Limited
- Design Complexity Limited
- Performance Limited
- High Power Consumption
- High Per-Unit Cost

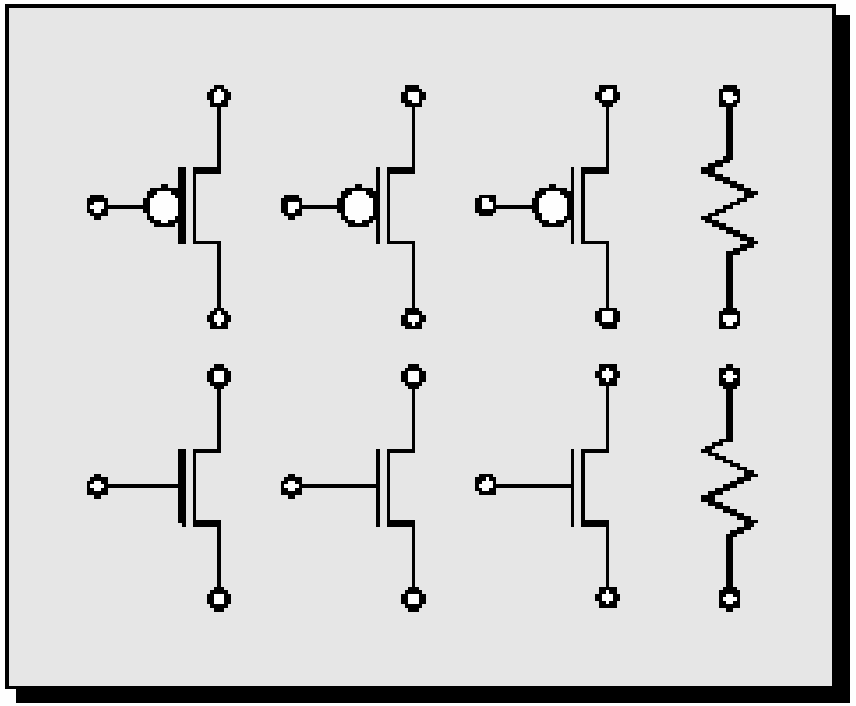
- Difficult to Design
- Long Development Time
- High NRE Costs
- Support Large Designs
- Support Complex Designs
- High Performance
- Low Power Consumption
- Low Per-Unit Cost (at high volume)

Structured ASIC's Combine the Best of Both Worlds

# Structured ASIC Architectures

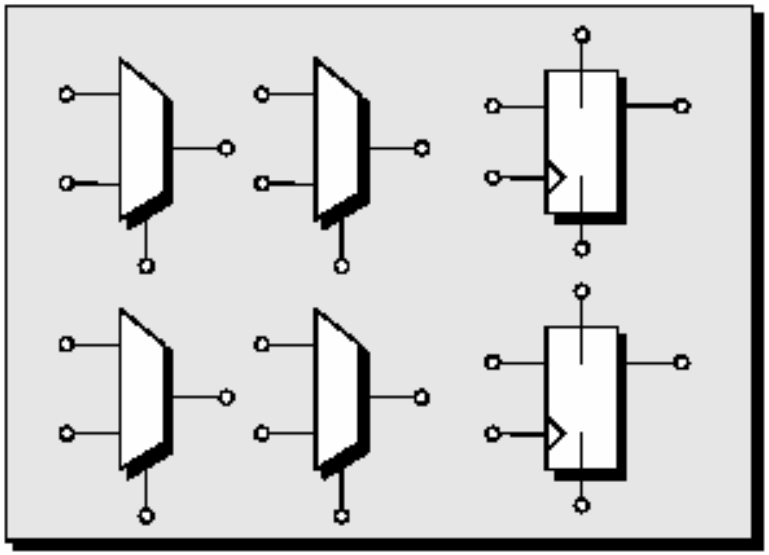
*Fine-Grained*

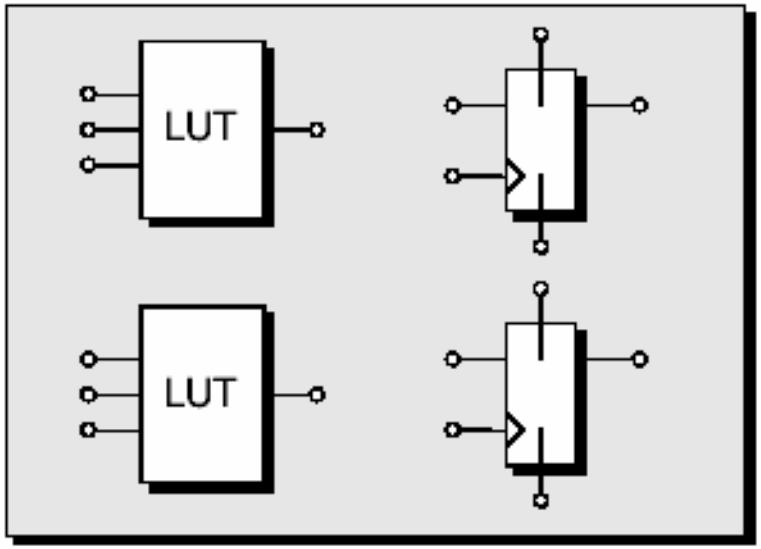
- Structured elements contain unconnected discrete components
- Could include transistors, resistors, and others



# Structured ASIC Architectures
## *Medium-Grained*

- Structured elements contain generic logic
- Could include gates, MUX's, LUT's or flip-flops





# Structured ASIC Architectures
## *Hierarchical*

- Use mini structured elements that contain only gates, MUX's, and LUT's
- It does not contain storage elements like flip-flops
- This mini element is then combined with registers or flip-flops

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## *Hierarchical*

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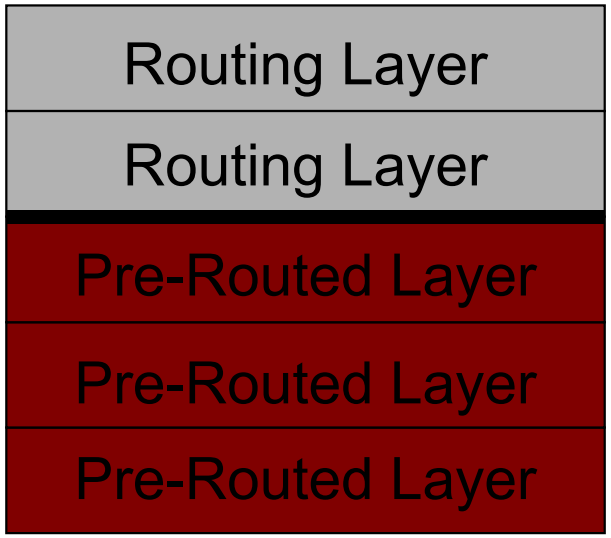
# Architecture Comparison

- Fine-grained requires many connections in and out of a structured element
- Higher granularities reduce connections to the structured element but decreases the functionality it can support
- Clearly, each individual design will benefit differently at varying granularities

# Structured ASIC Advantages

- Largely Prefabricated
  - Components are “almost” connected in a variety of predefined configurations
  - Only a few metal layers are needed for fabrication
  - Drastically reduces turnaround time



# Structured ASIC Advantages

- Easier and faster to design than standard cell ASIC's
  - Multiple global and local clocks are prefabricated
  - No skew problems that need to be addressed
  - Signal integrity and timing issues are inherently addressed

# Structured ASIC Advantages

- Capacity, performance, and power consumption closer to that of a standard cell ASIC
- Faster design time, reduced NRE costs, and quicker turnaround
- Therefore, the per-unit cost is reasonable for several hundreds to 100k unit production runs

# Structured ASIC Disadvantages

- Lack of adequate design tools
  - Expensive
  - Altered from traditional ASIC tools
- These new architectures have not yet been subject to formal evaluation and comparative analysis
  - Tradeoffs between 3-, 4-, and 5-input LUT's
  - Tradeoffs between sizes of distributed RAM

# Technology Comparison

- Generally speaking
  - 100:33:1 ratio between the number of gates in a given area for standard cell ASIC's, structured ASIC's, and FPGA's, respectively
  - 100:75:15 ratio for performance (based on clock frequency)
  - 1:3:12 ratio for power

# Design Tools

- Many companies are using existing standard cell-based CAD tools
  - They add product specific placement tools
  - To maximize benefits, we need CAD tools designed specifically for structured ASIC's
  - Need updated algorithms to exploit the modularity of structured ASIC's
  - Clock aware design
- Need architectural evaluation and analysis tools