Perancangan Elektronika Berbantuan Komputer

Proses Desain

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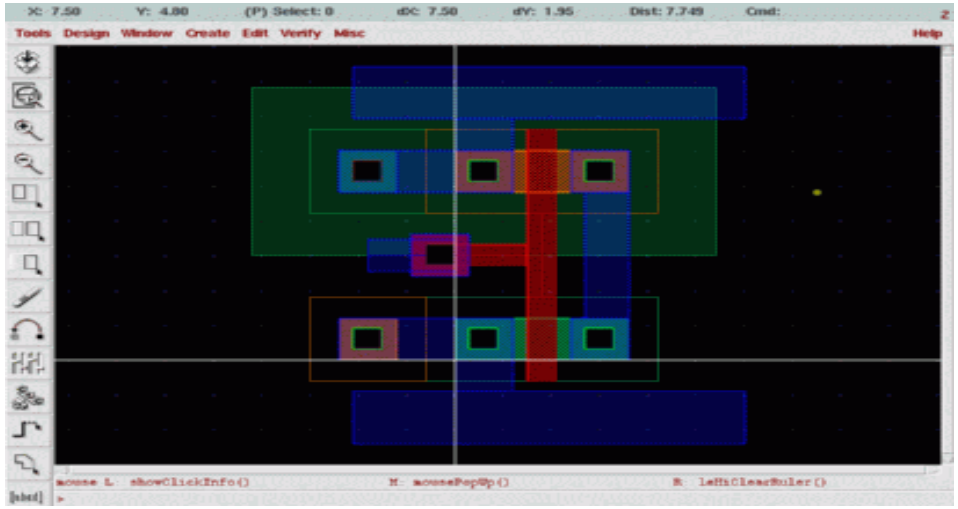
Issues

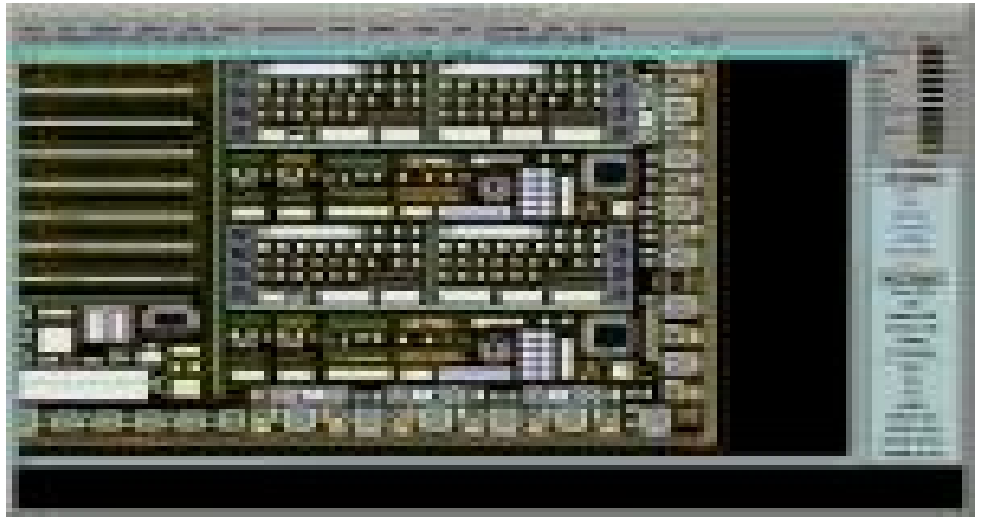
- Software Tools Design
- CHIP Fabrication
- Cost
- How to design the transistor circuits into the CHIP

Software Tools Design

- LASI,MAGIC,DREAI
- MAX,MyCAD LAYED
- Cadence
- Synopsis



- Mentor Graphics



Pengguna Mentor Graphics

INDONESIA

Gunadarma University

KOREA REPUBLIC OF

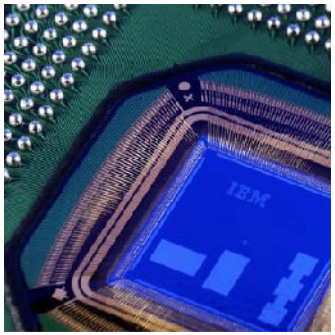
Information & Communication Univ.
INFORMATION&COMM.UNIVERSITY
KAIST
KAIST Tara Lab
KAIST/IDEC
Korea University
Kyunghee University
NamSeoul University
POSTECH
SEOUL NATIONAL UNIVERSITY
University of Ulsan
YONGSEI UNIVERSITY
YONSEI UNIVERSITY

MALAYSIA

Universiti Teknologi MARA
University Technology PetroAmericass
Kolej Bandar Utama
InterAmericastioAmericasl Islamic University
Mimos University PacRimogram
Kolej Universiti Kejuruteraan Utara
University Science Malaysia

CHIP Fabrication

- CMP-TIMA, France
- TSMC, Taiwan
- NEC, Japan
- Mosis, USA
- Mimos,Malaysia ?
- Etc

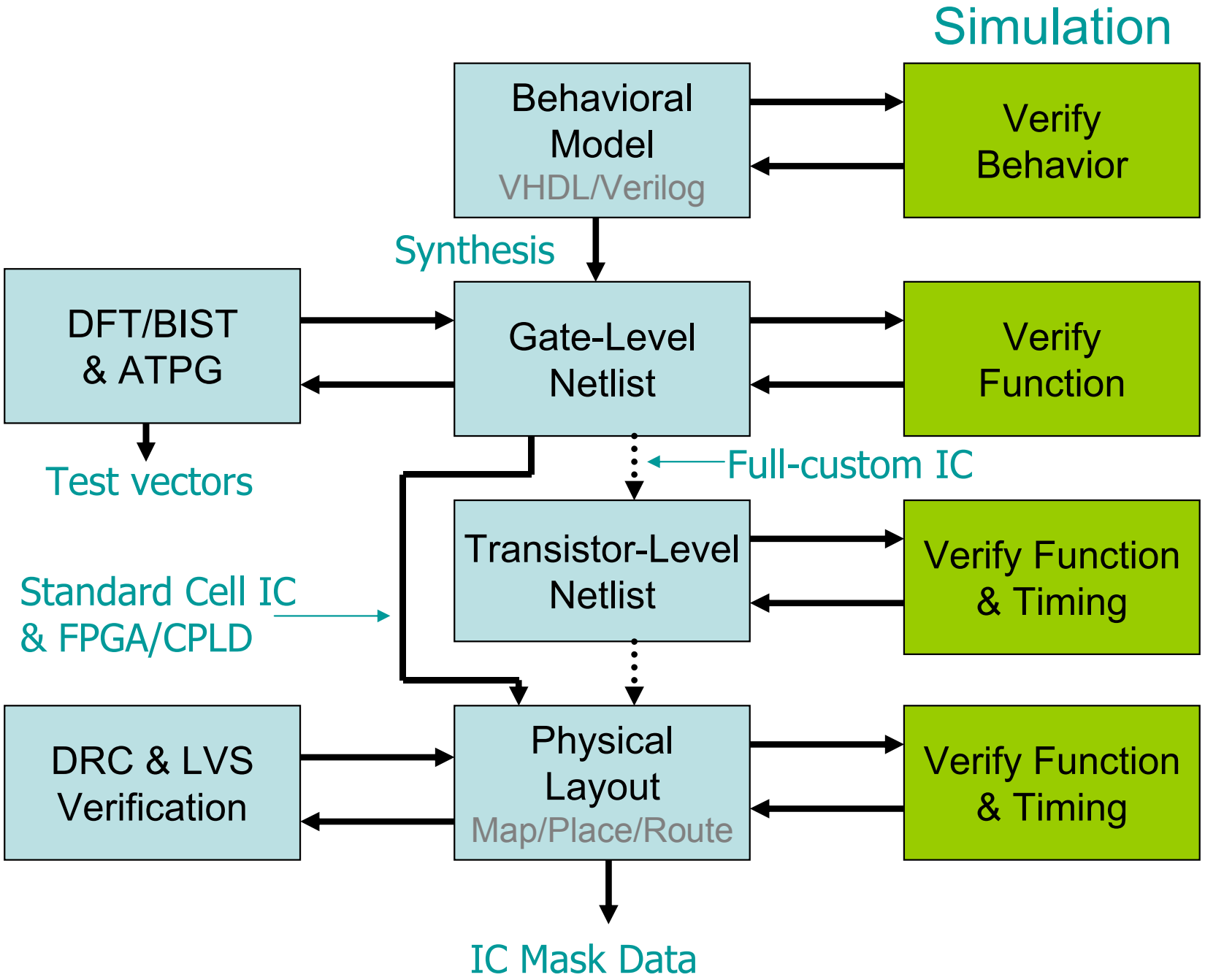


Cost

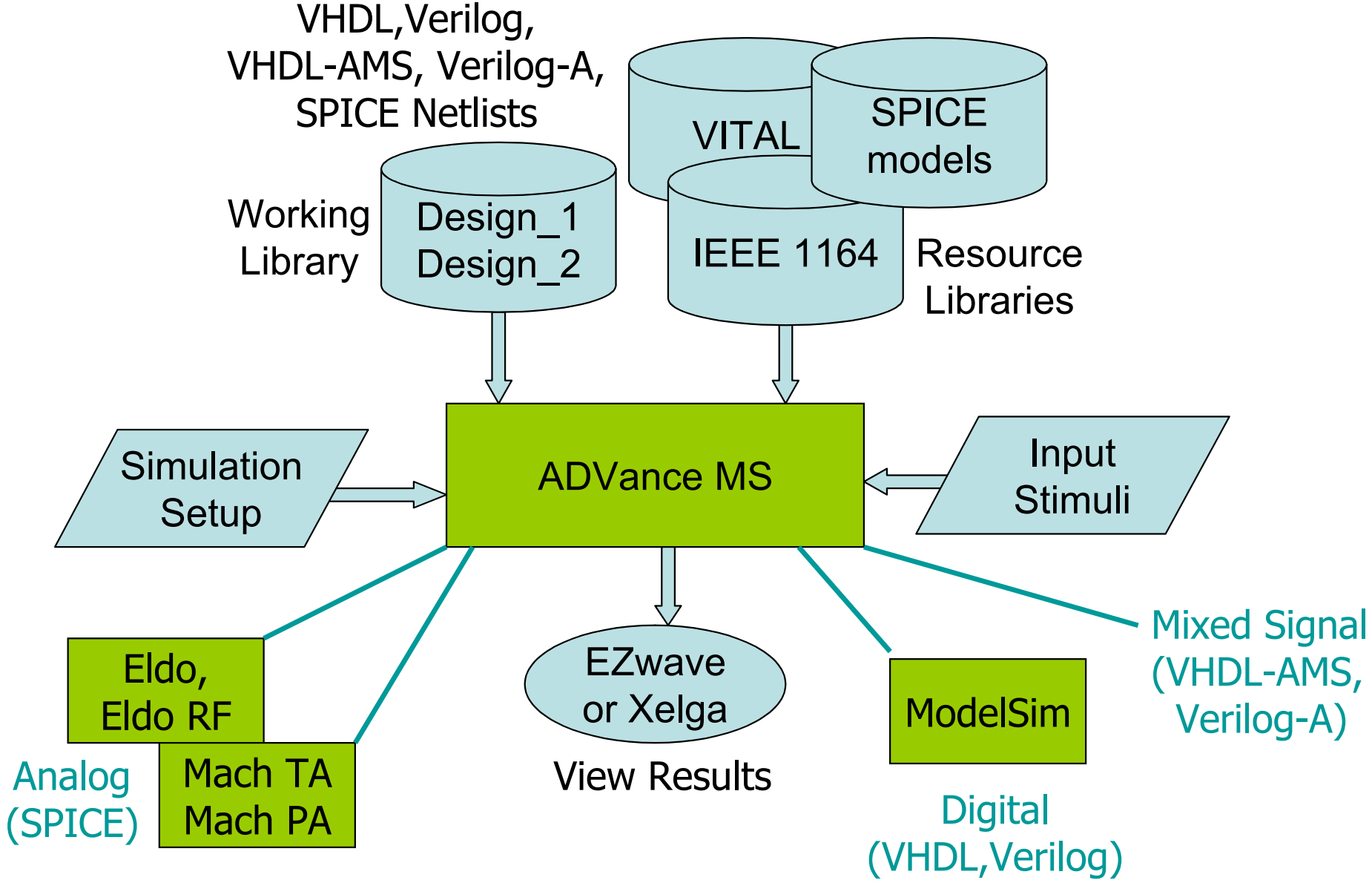
- Austria Micro Systems
  - 0.6 CMOS CUP — 390 Euro/mm^2
  - 0.35 CMOS C35B4C3 — 650 Euro/mm^2
- STMicroelectronics
  - 0.18 CMOS HCMOS8D — 990 Euro/mm^2
  - 0.12 CMOS HCMOS9GP — 2500 Euro/mm^2
  - 90 nm CMOS CMOS090 — 5000 Euro/mm^2

Mentor Graphics Simulation Tools for ASIC Design

ASIC Design Flow



ADVance MS
Digital, Analog, Mixed-Signal Simulation

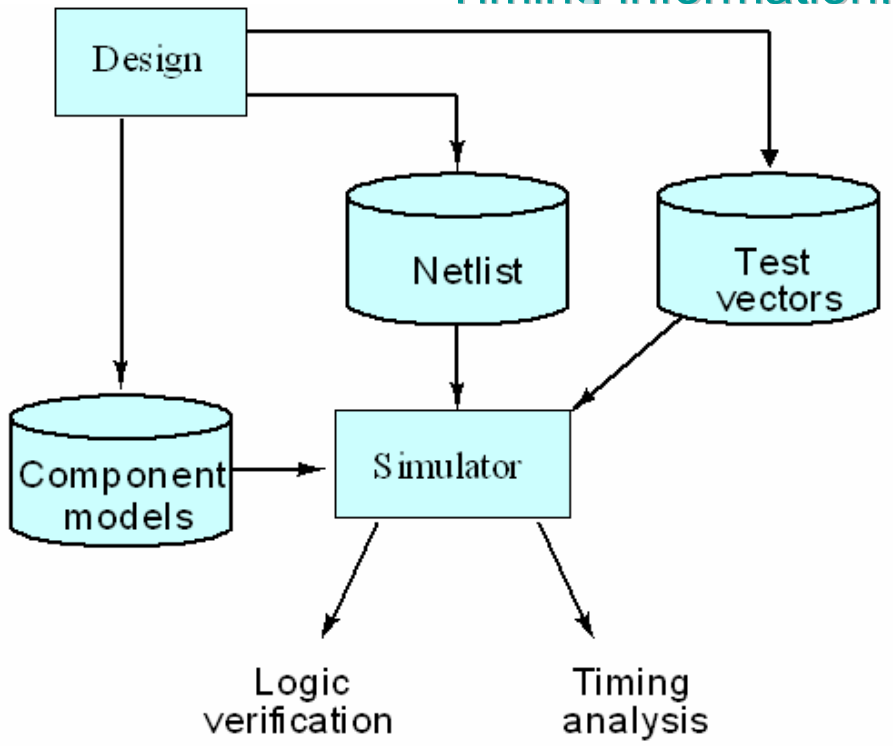


Mentor Graphics Legacy Simulators

- Originally designed for PCB design
  - Quicksim II : digital, gate-level simulation
    - Invoke : *quicksim*
    - ASIC Design Kit : *adk_quicksim*
    - Xilinx FPGA : *pld_quicksim*, Altera : *max2_quicksim*
  - Quicksim Pro : mixed schematic & HDL
    - Uses both Quicksim II and Modelsim EE
    - Invoke: *qspro*
  - Accusim : analog simulation (SPICE)
    - Invoke : *adk_accusim*

Basic simulation environment

-Behavioral description,
-Circuit structure/netlist,
-Timing information.



-Generic,
-Technology-specific

-Digital values,
-Analog voltages/ currents,
-Waveforms

Results listings, graphical waveforms,
Reports of measurements, result checks,
constraint violations, etc.

Mentor Graphics ASIC Design Kit (ADK)

- ASIC technology files & standard cell libraries
  - AMI: ami12, ami05 (1.2, 0.5 µm)
  - TSMC: tsmc035, tsmc025, tsmc018 (0.35, 0.25, 0.18 µm)

- IC flow & DFT tool support files:
  - Simulation
    - VHDL/Verilog/Mixed-Signal models *(Modelsim/ADVance MS)*
    - Analog (SPICE) models *(Eldo/Accusim)*
    - Post-layout verification *(Mach TA)*
    - Digital schematic *(Quicksim II, Quicksim Pro)* (exc. tsmc025,tsmc018)
  - Synthesis library of std. cells *(LeonardoSpectrum)*
  - Design for test & ATPG *(DFT Advisor, Flextest/Fastscan)*
  - Schematic capture *(Design Architect-IC)*
  - IC physical design (standard cell & custom)
    - Floorplan, place & route *(IC Station)*
    - Design rule check, layout vs schematic, parameter extraction *(Calibre)*

HDLs in Digital System Design

- Model and document digital systems
  - Hierarchical models
    - System, RTL (Register Transfer Level), gates
  - Different levels of abstraction
    - Behavior, structure
- Verify circuit/system design via simulation
  - Modelsim EE (VHDL, Verilog, System C)
  - ADVance MS (above + VHDL-AMS, Verilog-A)
- Synthesize circuits from HDL models
  - Leonardo (Synopsis)

```
-- count4.vhd     4-bit parallel-load synchronous counter
LIBRARY ieee;
USE ieee.std_logic_1164.all; USE ieee.numeric_std.all;

ENTITY count4 IS
  PORT (clock,clear,enable,load_count : IN STD_LOGIC;
        D: IN  unsigned(3 downto 0);
        Q: OUT unsigned(3 downto 0));
END count4;

ARCHITECTURE rtl OF count4 IS
SIGNAL int : unsigned(3 downto 0);
BEGIN
   PROCESS(clear, clock, enable)
   BEGIN
      IF (clear = '1') THEN
           int <= "0000";
      ELSIF (clock'EVENT AND clock='1') THEN
           IF (enable = '1') THEN
               IF (load_count = '1') THEN
                    int <= D;
               ELSE
                    int <= int + "01";
               END IF;
           END IF;
      END IF;
  END PROCESS;
  Q <= int;
END rtl;
```

Typical VHDL behavioral model

flowchart proses disain

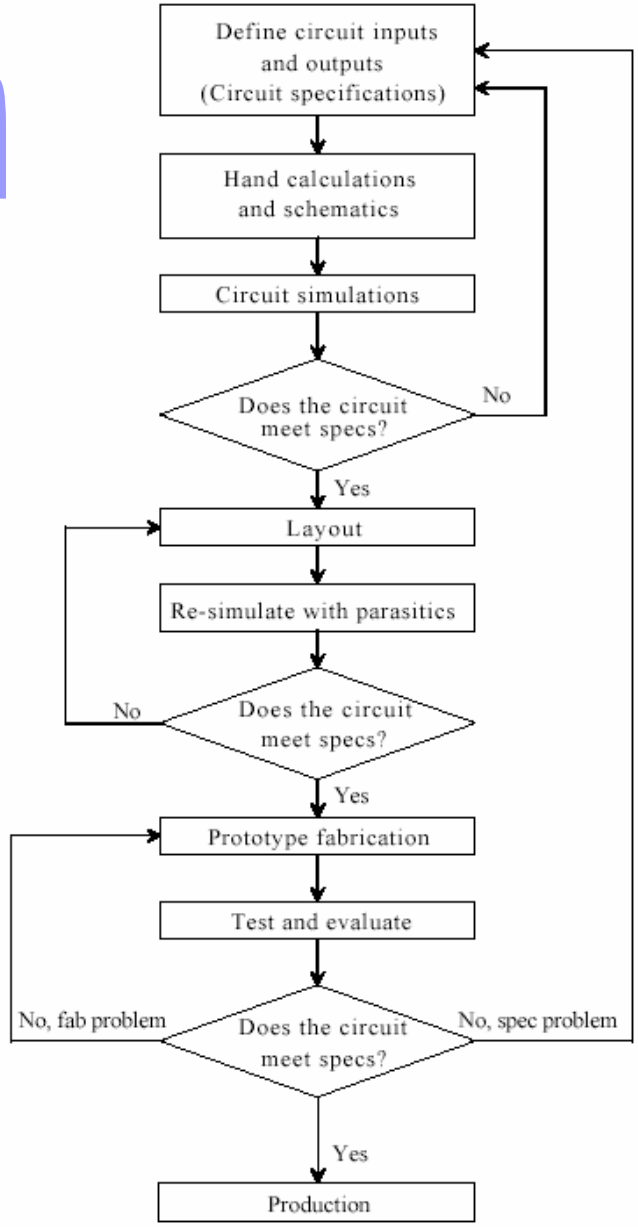
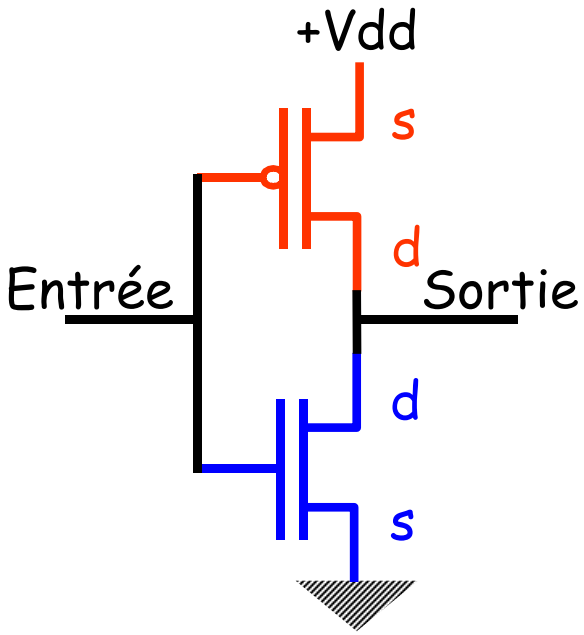


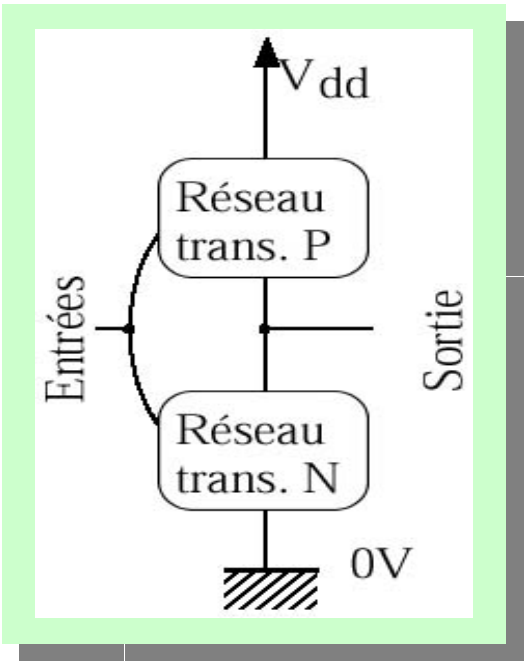
Figure 1.1 Flowchart for the CMOS IC design process.

Structures Complementary MOS

CMOS = NMOS + PMOS

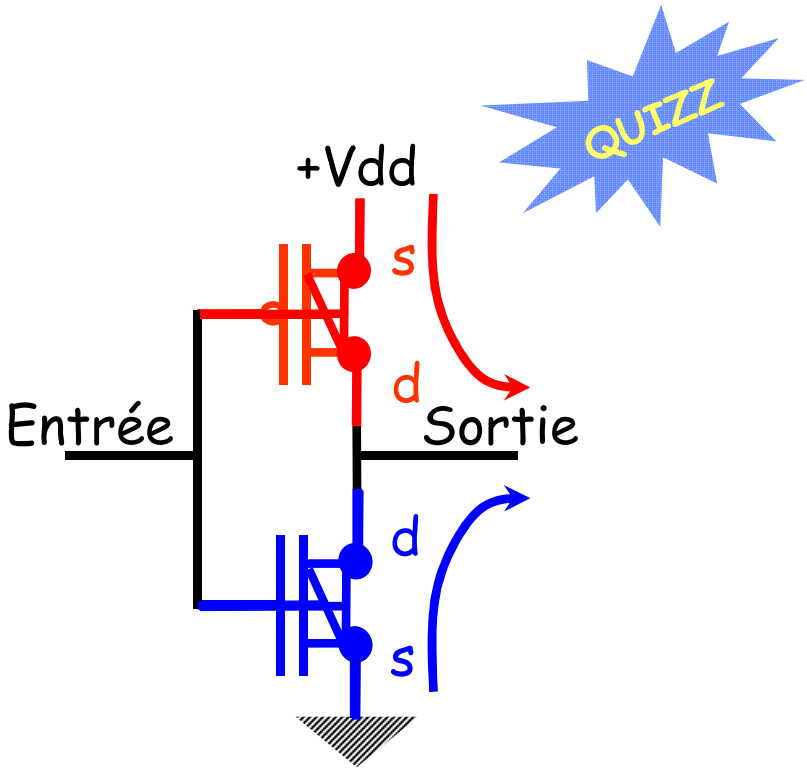
La structure CMOS permet de construire l'élément de base de la logique à effet de champ : l'inverseur





Comment ça marche ?

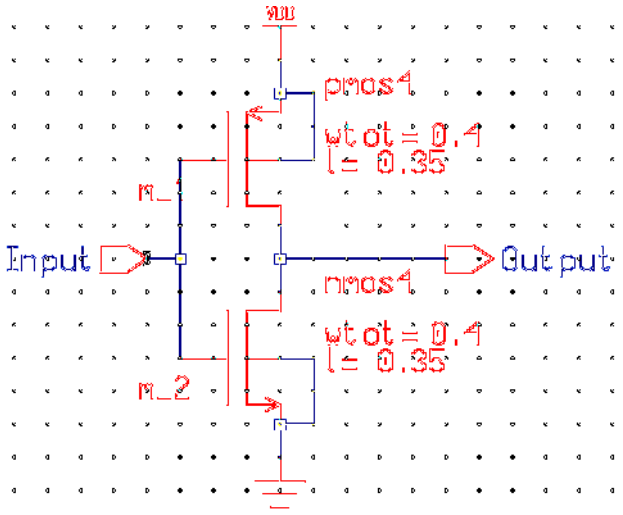
Un inverseur CMOS peut être vu comme un double interrupteur en série



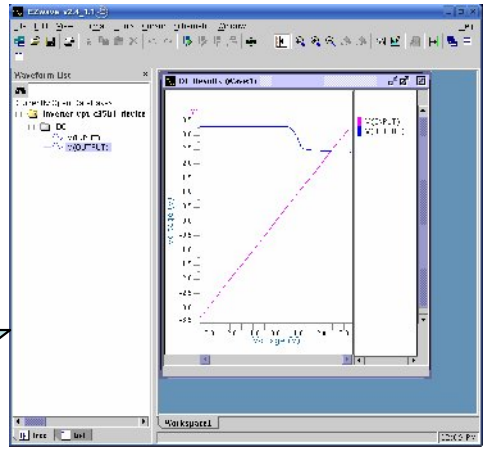
ENTREE = 0
PMOS : Conducteur / ~~Bloqué~~
NMOS : ~~Conducteur~~ / Bloqué
SORTIE = 1

ENTREE = 1
PMOS : ~~Conducteur~~ / Bloqué
NMOS : Conducteur / ~~Bloqué~~
SORTIE = 0

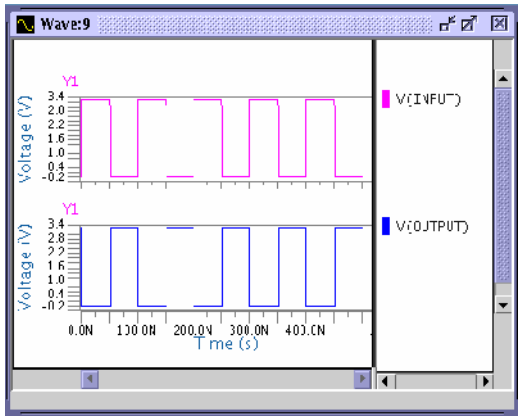
Process Visual



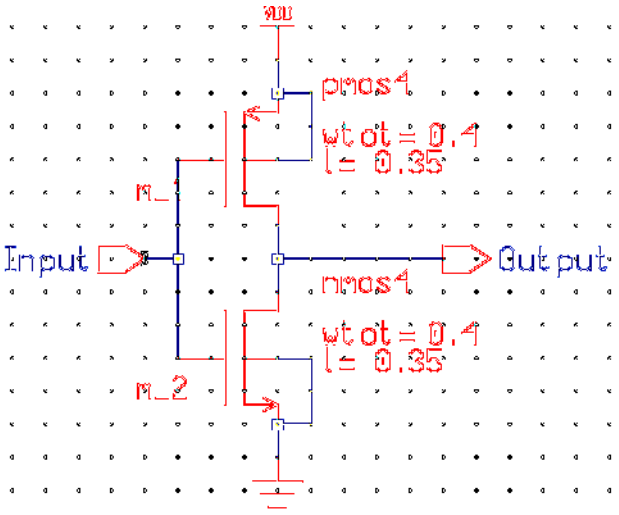
Disain skema



Hasil Simulasi



Process Visual



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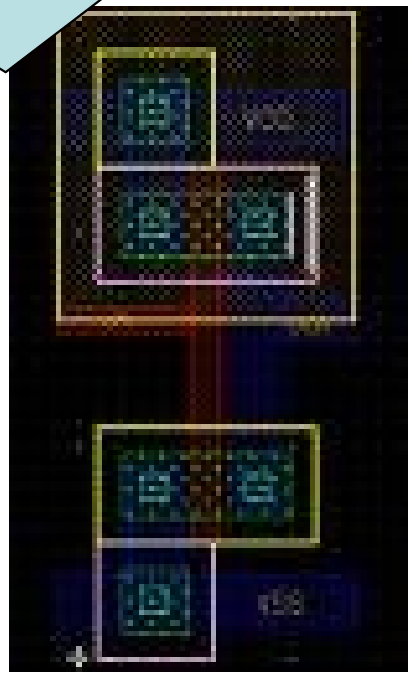
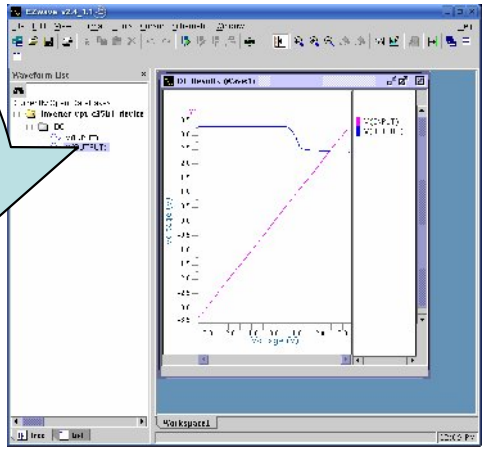
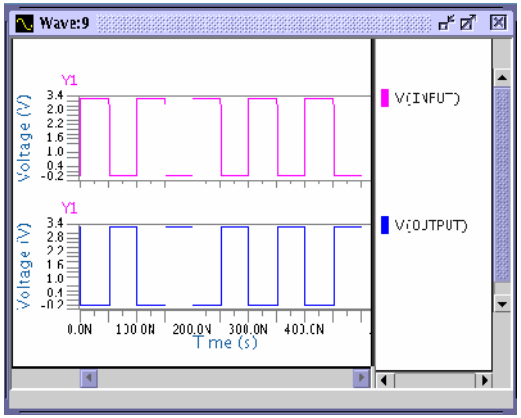


Disain Layout



Hasil Simulasi



Layout Siap Untuk Difabrikasi