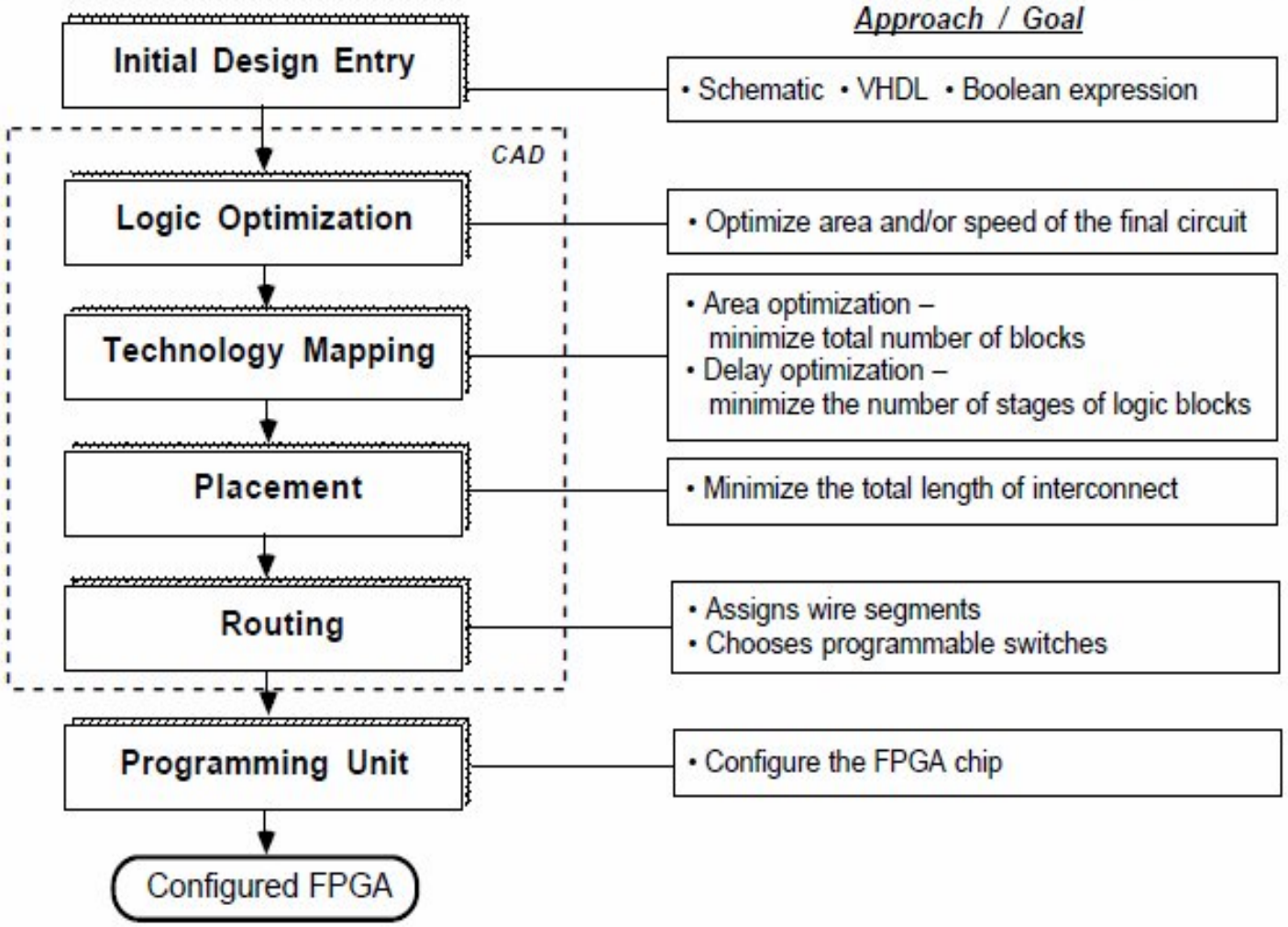
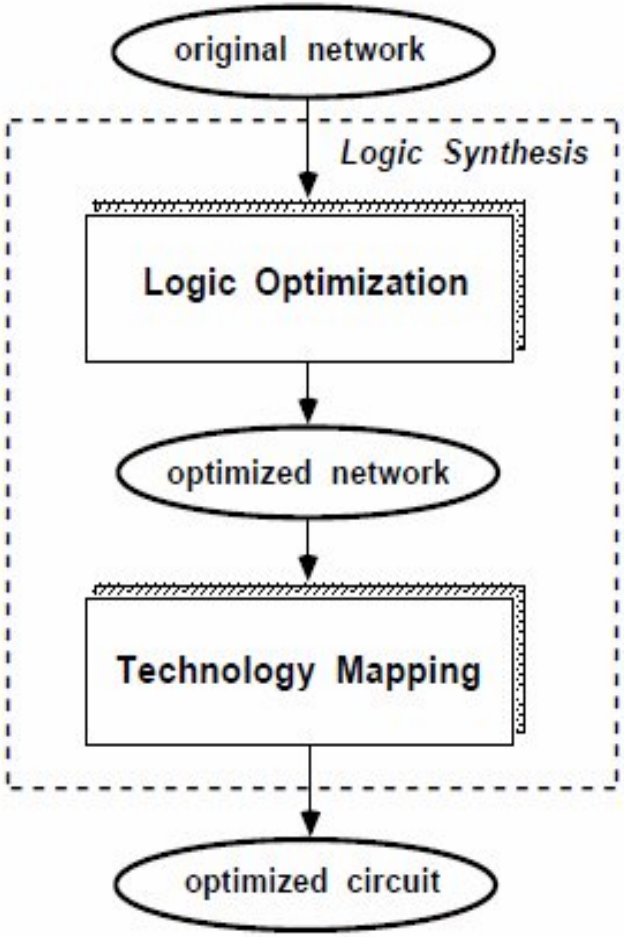
FPGA

Eri Prasetyo
Universitas Gunadarma

FPGA Implementation Process

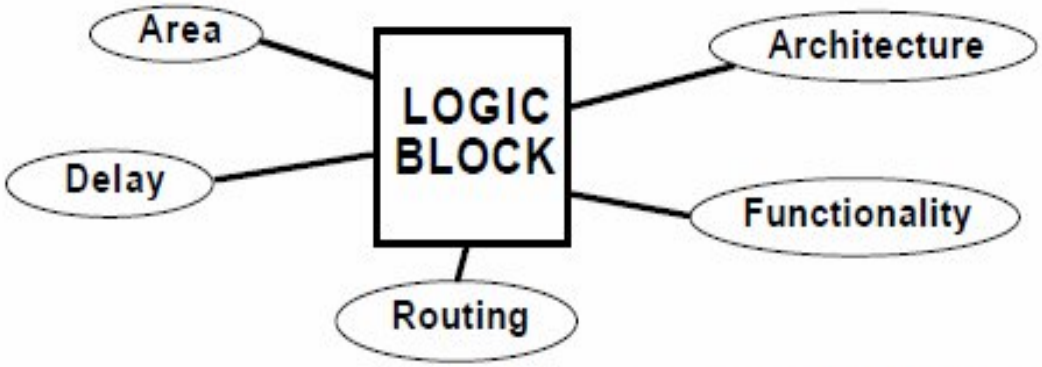


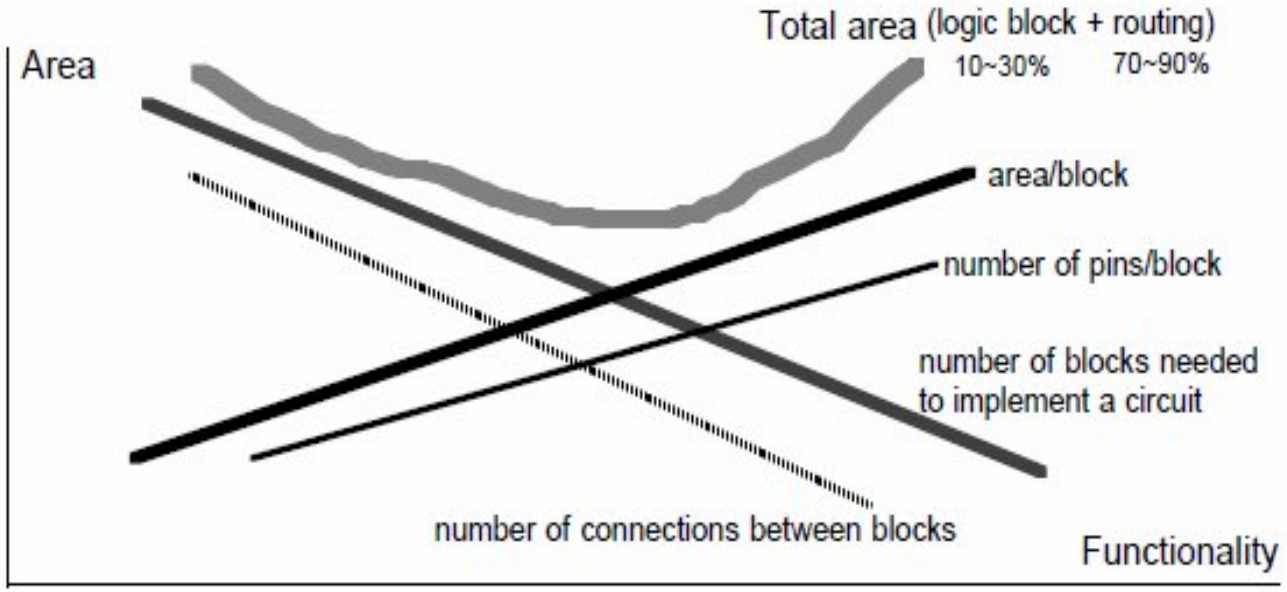
Logic Optimization and Technology Mapping



- **Logic optimization**
  - Technology independent
  - Redundancy removal
  - Common subexpression elimination
  - Don't-care exploitation
- **Technology mapping**
  - Technology and architecture dependent
  - Optimized circuit considering both area and delay
  - Library-based
  - Lookup table
  - Multiplexer-based

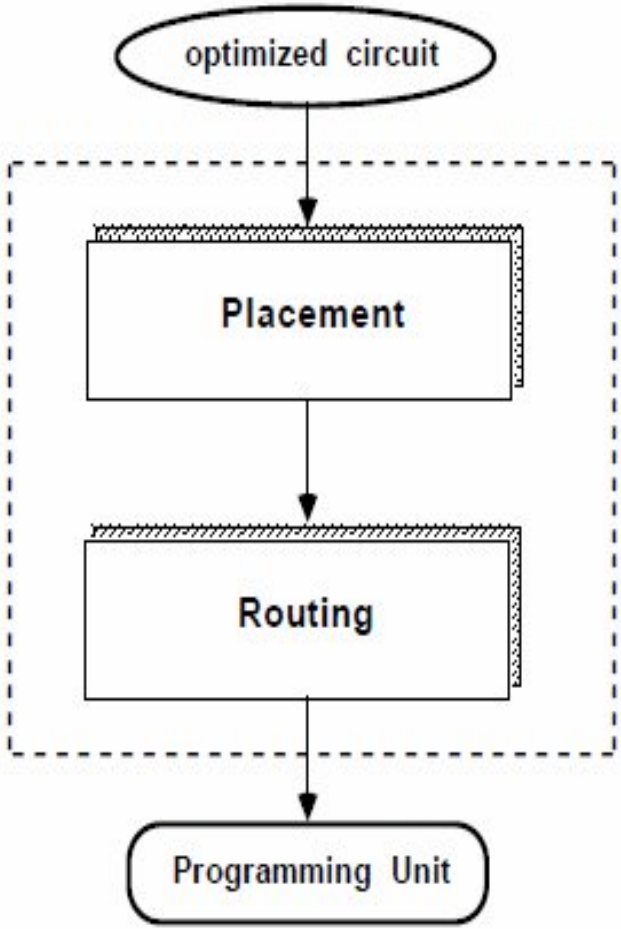
Logic Block Architecture





Logic Block Functionality vs Area-Efficiency

Placement and Routing



- **Placement**
  - Assign each Logic Cell to a specific location in the FPGA
  - Well developed techniques
  - Similar to other technologies
- **Routing**
  - Achieve interconnections among the Logic Cells by selecting wire segments and routing switches
  - Routing architectures
    - Row-based FPGA: only horizontal routing channels
    - Symmetrical FPGA: both vertical and horizontal routing channels

Generic FPGA Development Cycle