

# Outline

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- Introduction – *“Is there a limit?”*
- Transistors – *“CMOS building blocks”*
- Parasitics – *“The [un]desirables”*
- The CMOS inverter – *“A masterpiece”*
- Gates – *“Just like LEGO”*
- **Sequential circuits – *“Time also counts!”***
- Storage elements – *“A bit in memory”*
- Technology scaling – *“..., faster!”*
- Technology – *“Building an inverter”*

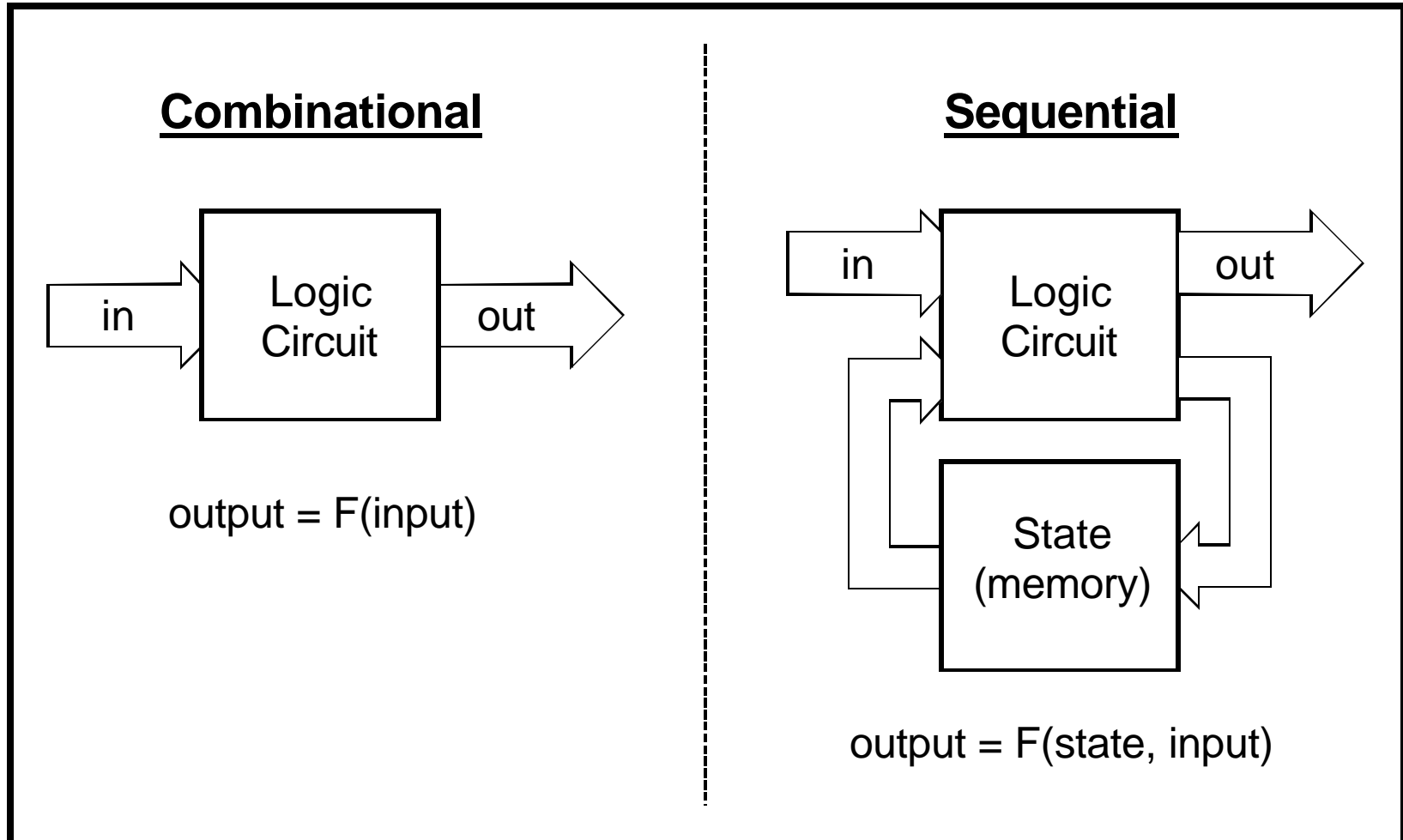
# Sequential circuits

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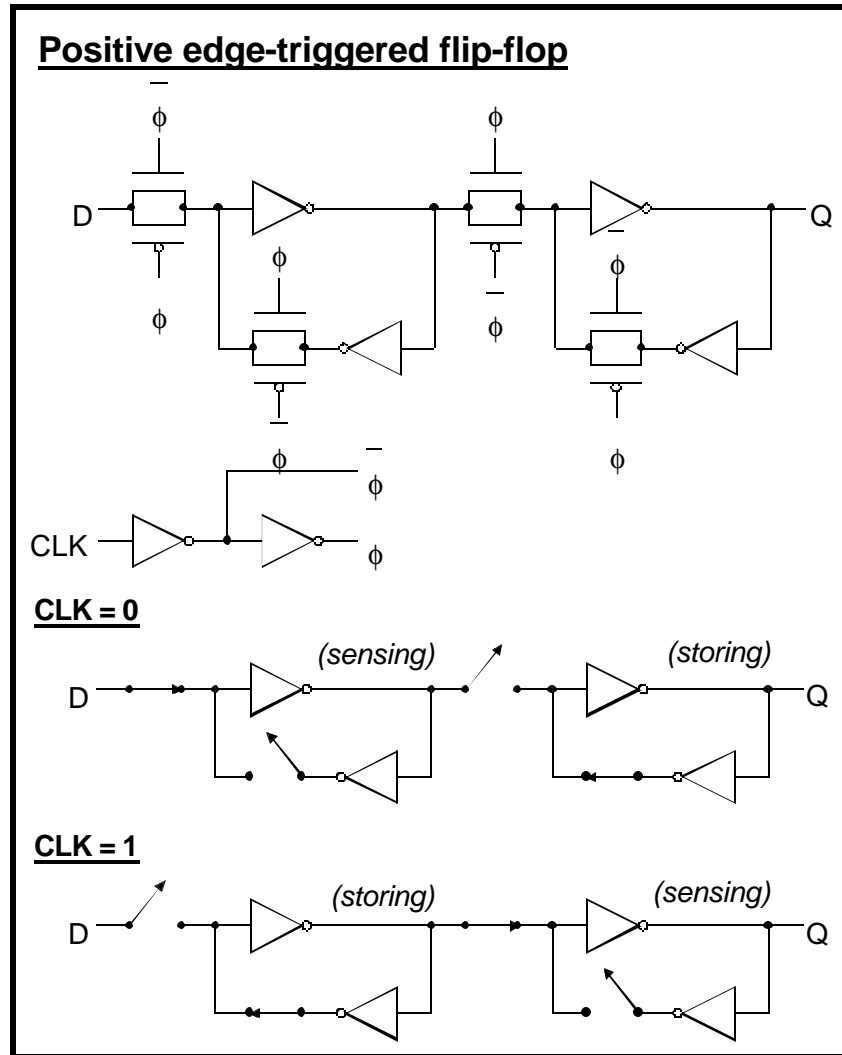
- Time in logic circuits
- D flip-flop
- State machine timing
- Interconnects
- Clock distribution

# “Time also counts”

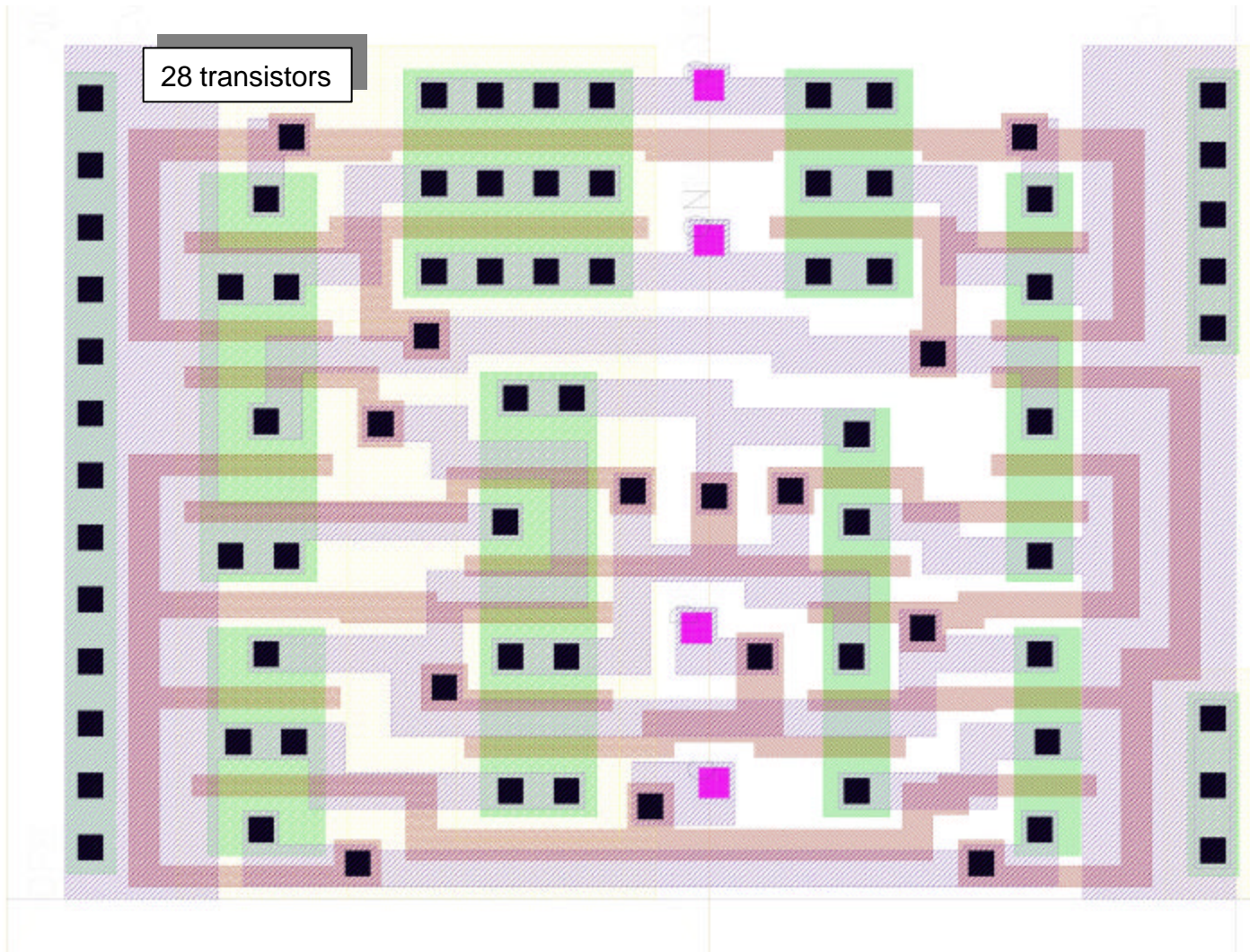
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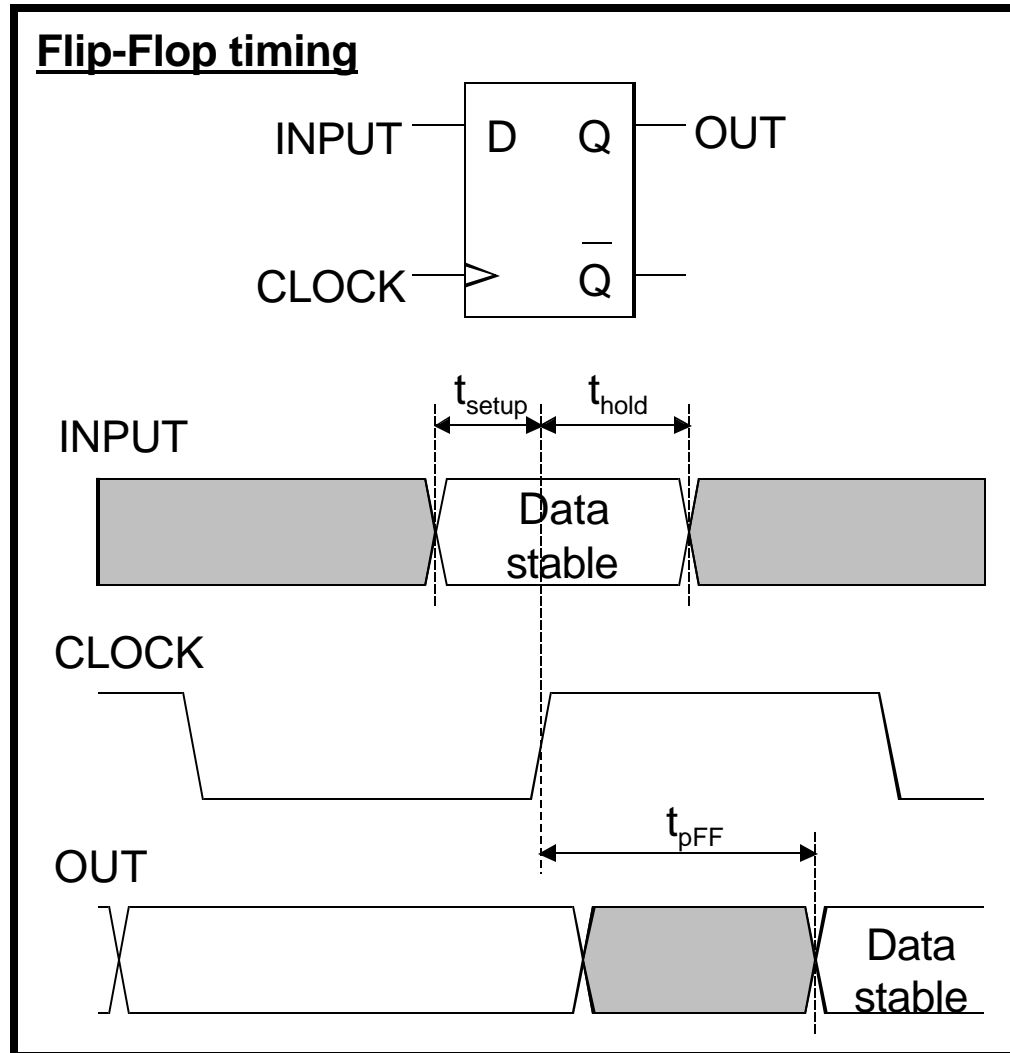
# D Flip-Flop



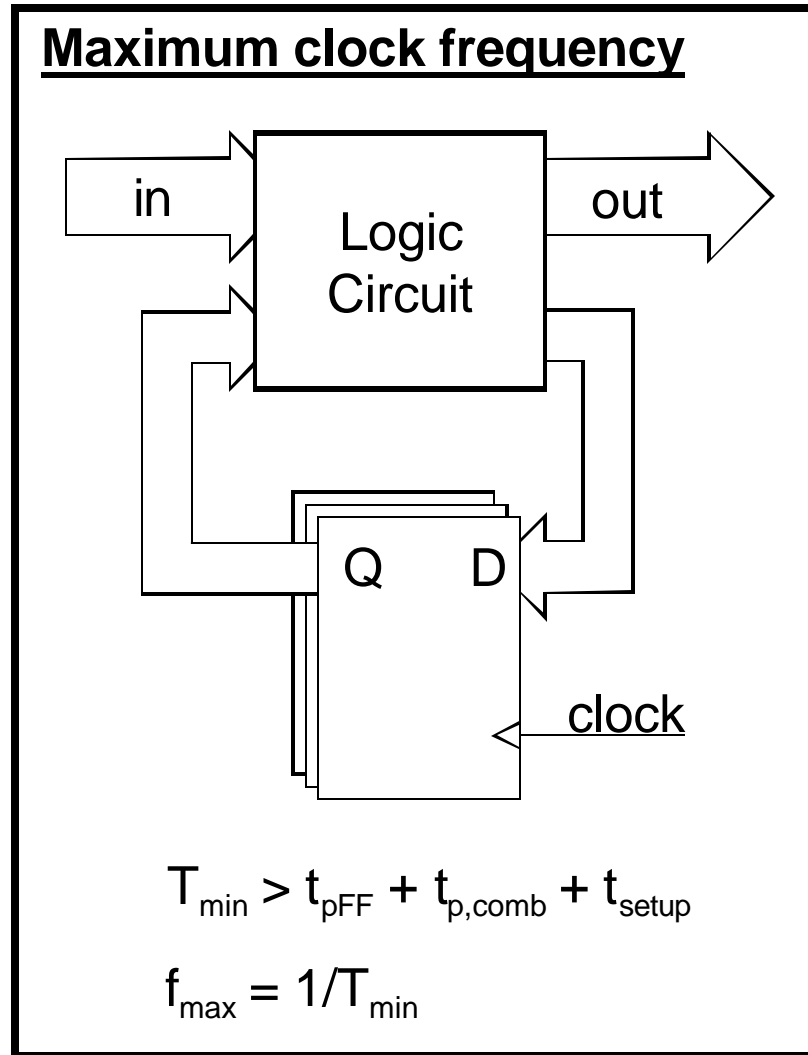
# D Flip-Flop



# State machine timing



# State machine timing



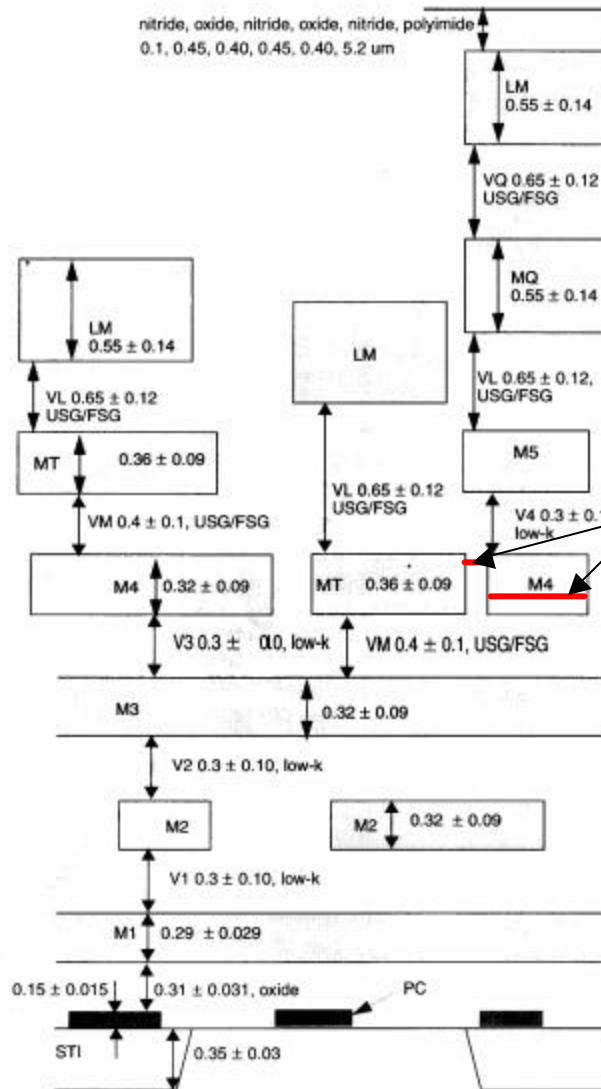
# Interconnects

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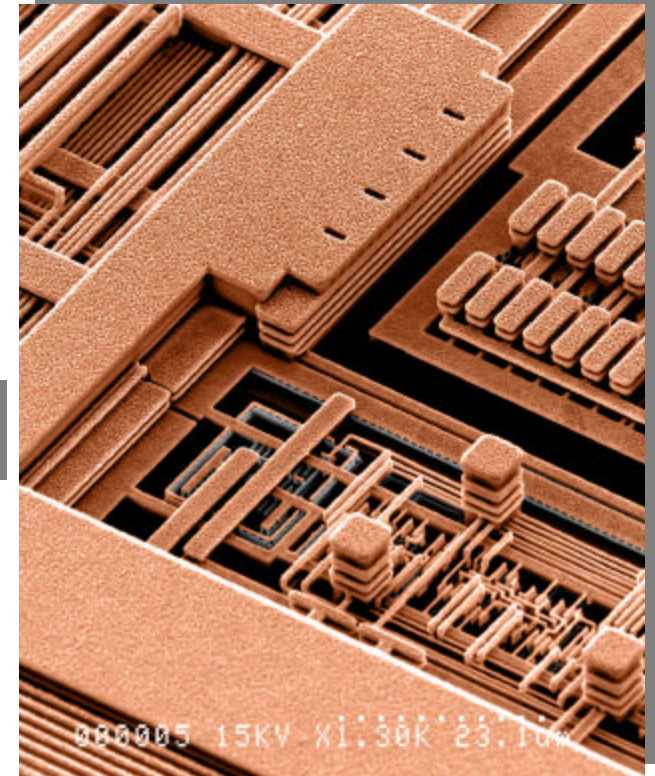
- The previous result assumes that signals can propagate instantaneously across interconnects
- In reality interconnects are metal or polysilicon structures with associated resistance and capacitance.
- That, introduces signal propagation delay that has to be taken into account for reliable operation of the circuit



# Interconnects



Minimum Pitch: 0.2 μm  
Minimum Width 0.2 μm



- § Capacitance to substrate becomes irrelevant
- § Capacitance to neighboring signal becomes dominating
- § Noise to neighboring signal also not negligible
- § Extraction for Timing simulation horribly complicated: tools absolutely mandatory

# Interconnects

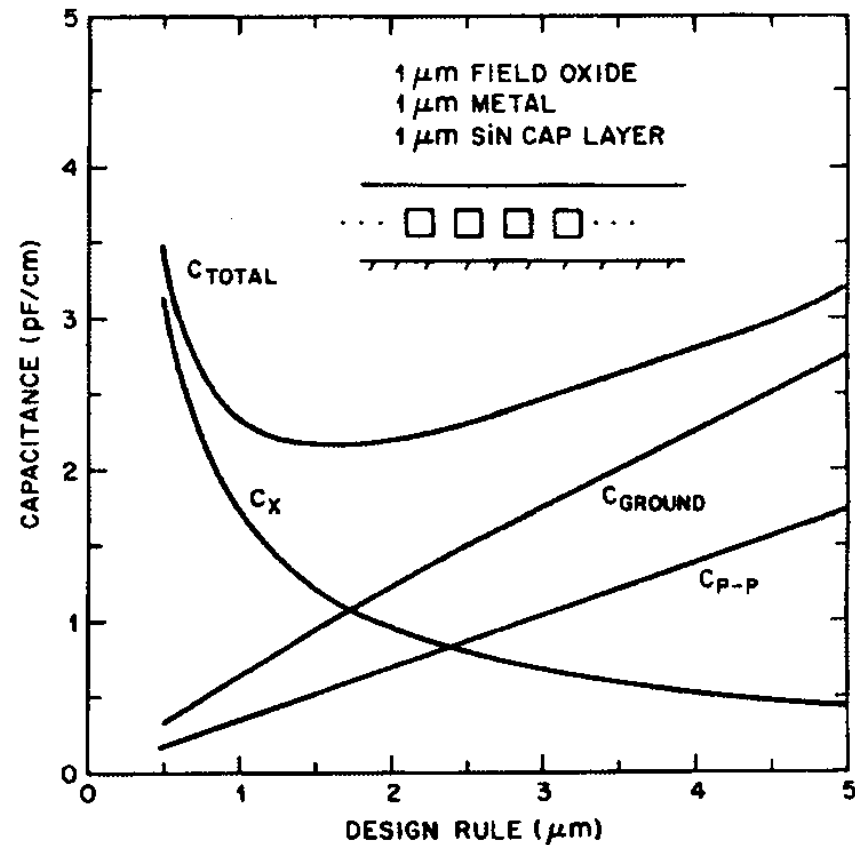
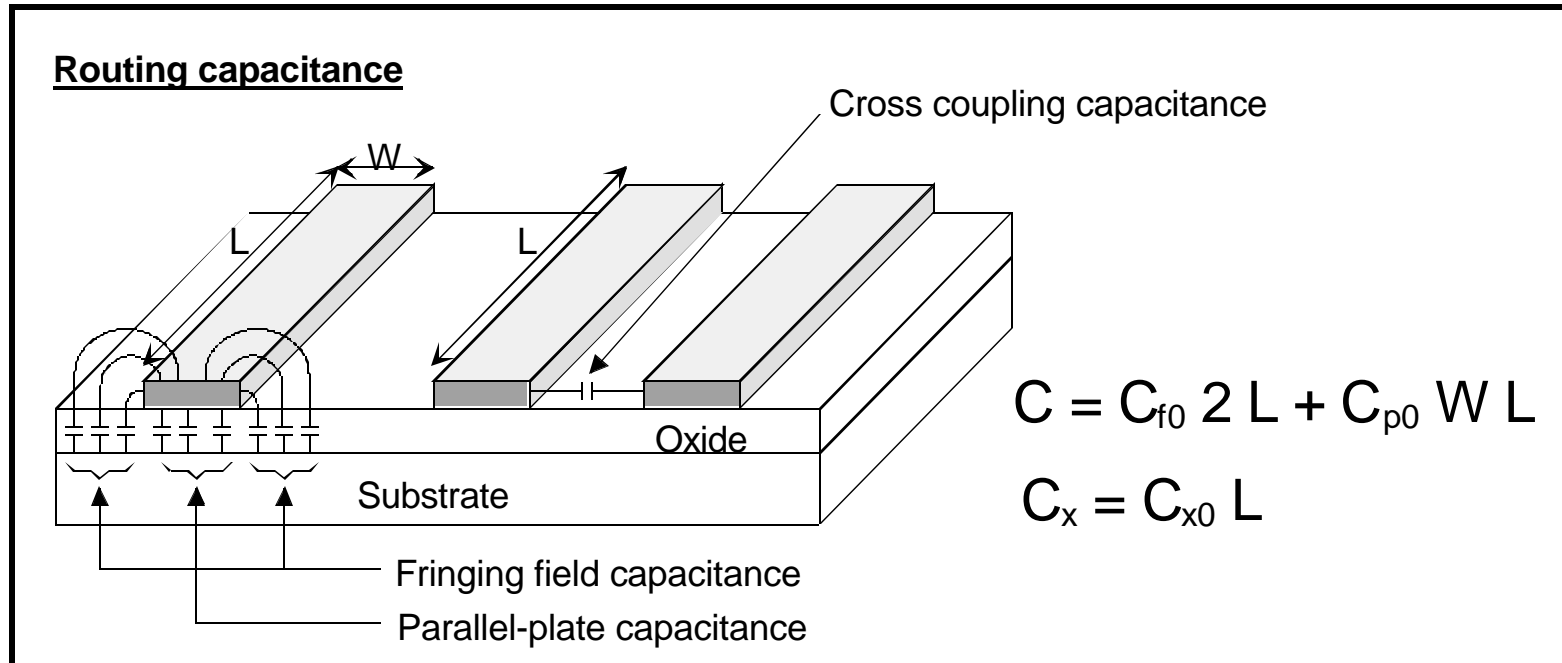


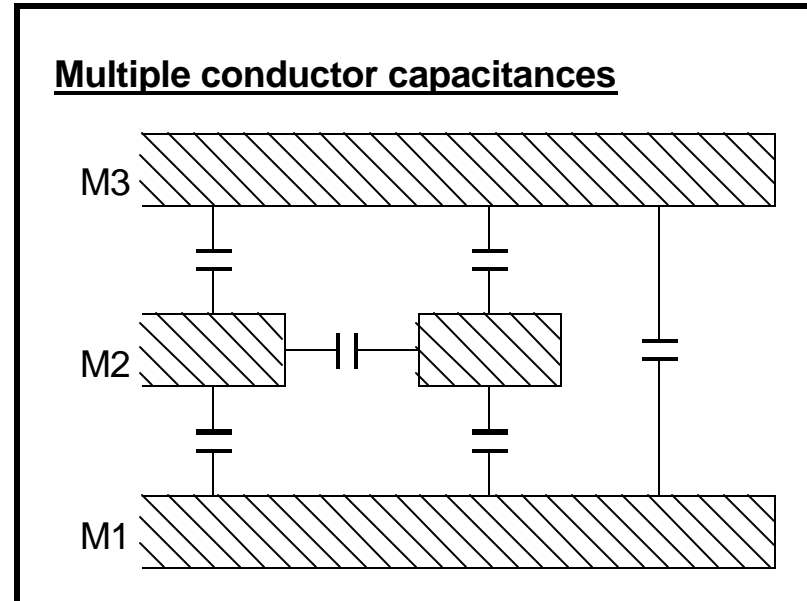
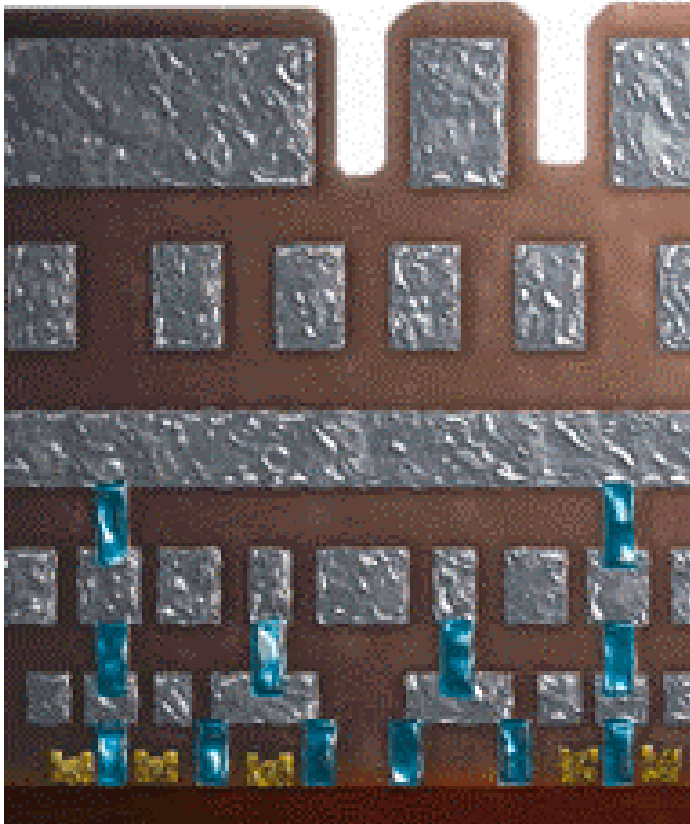
Figure 3.10: Interconnect capacitance including wire-to-wire capacitance [Schaper83]. (© 1983 IEEE)

# Interconnects



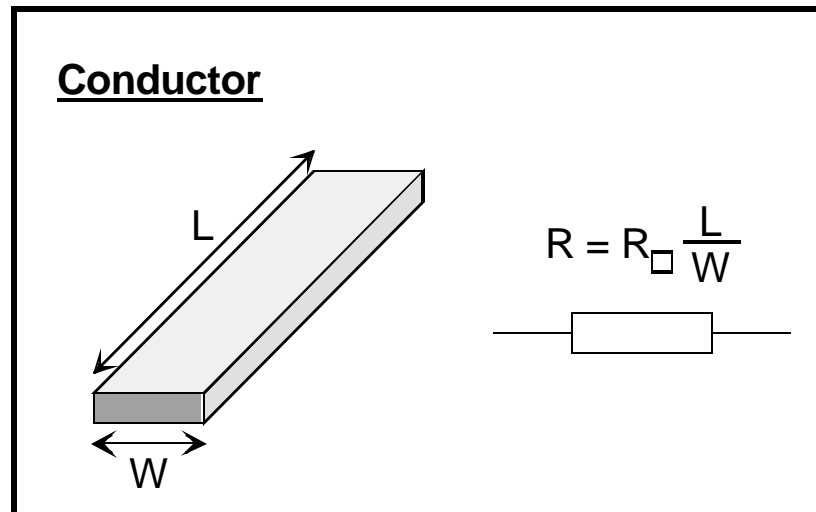
Interconnect layer	Parallel-plate (fF/ $\mu\text{m}^2$ )	Fringing (fF/ $\mu\text{m}$ )
Polysilicon to sub.	0.058	0.043
Metal 1 to sub.	0.031	0.044
Metal 2 to sub.	0.015	0.035
Metal 3 to sub.	0.010	0.033

# Interconnects



- Three dimensional field simulators are required to accurately compute the capacitance of a multi-wire structure

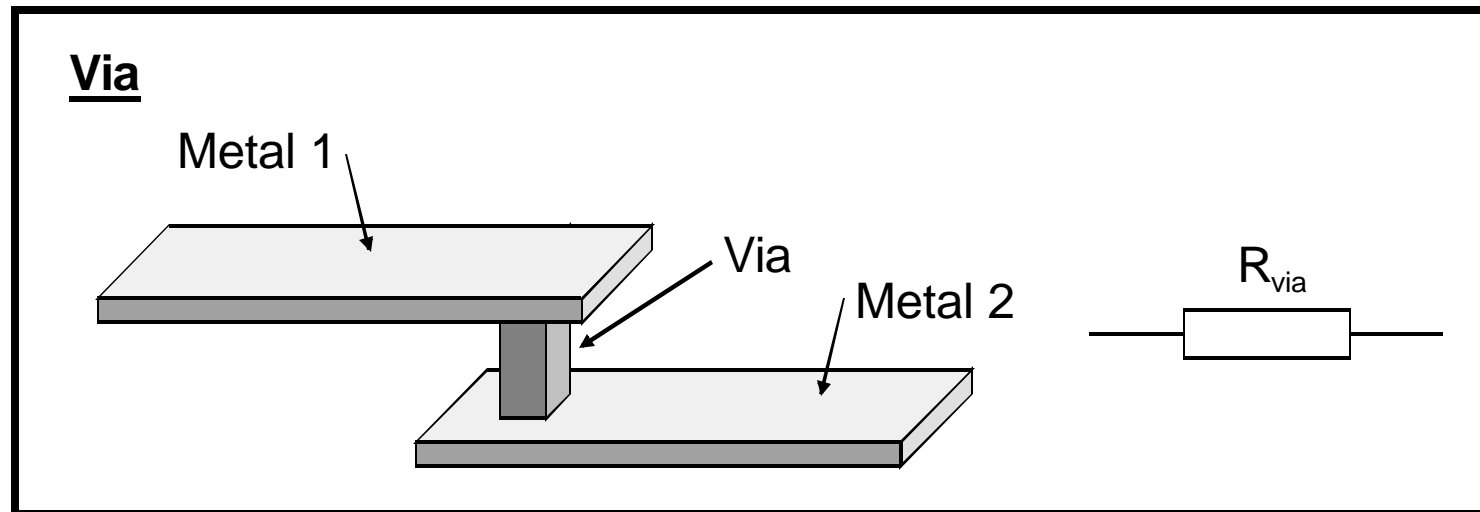
# Interconnects



Film	Sheet resistance ( $\Omega/\text{square}$ )
n-well	310
p+, n+ diffusion (salicided)	4
polysilicon (salicided)	4
Metal 1	0.12
Metal 2, 3 and 4	0.09
Metal 5	0.05

(Typical values for an advanced process)

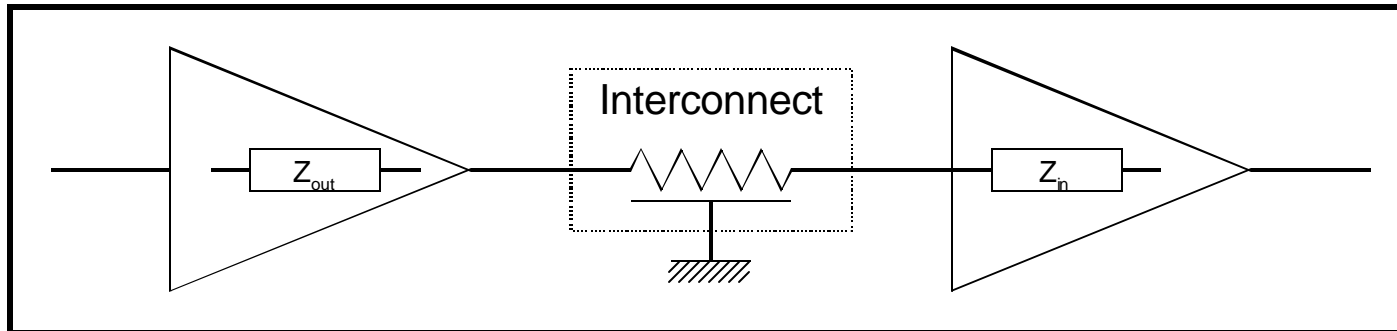
# Interconnects



- Via or contact resistance depends on:
  - The contacted materials
  - The contact area

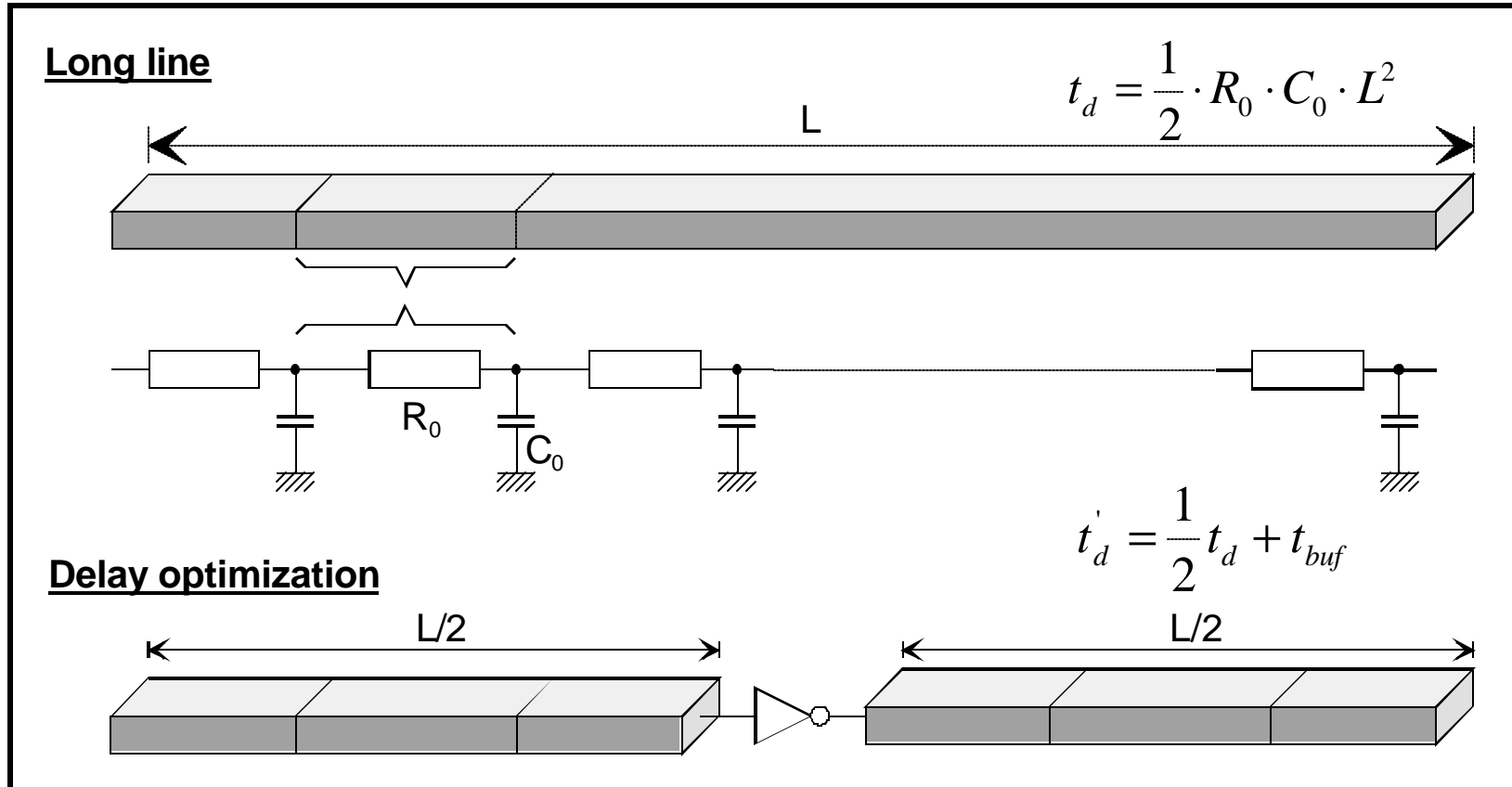
Via/contact	Resistance ( $\Omega$ )
M1 to n+ or p+	10
M1 to Polysilicon	10
V1, 2, 3 and 4	7

# Interconnects



- Delay depends on:
  - Impedance of the driving source
  - Distributed resistance/capacitance of the wire
  - Load impedance
- Distributed RC delay:
  - Can be dominant in long wires
  - Important in polysilicon wires (relatively high resistance)
  - Important in salicided wires
  - Important in heavily loaded wires

# Interconnects



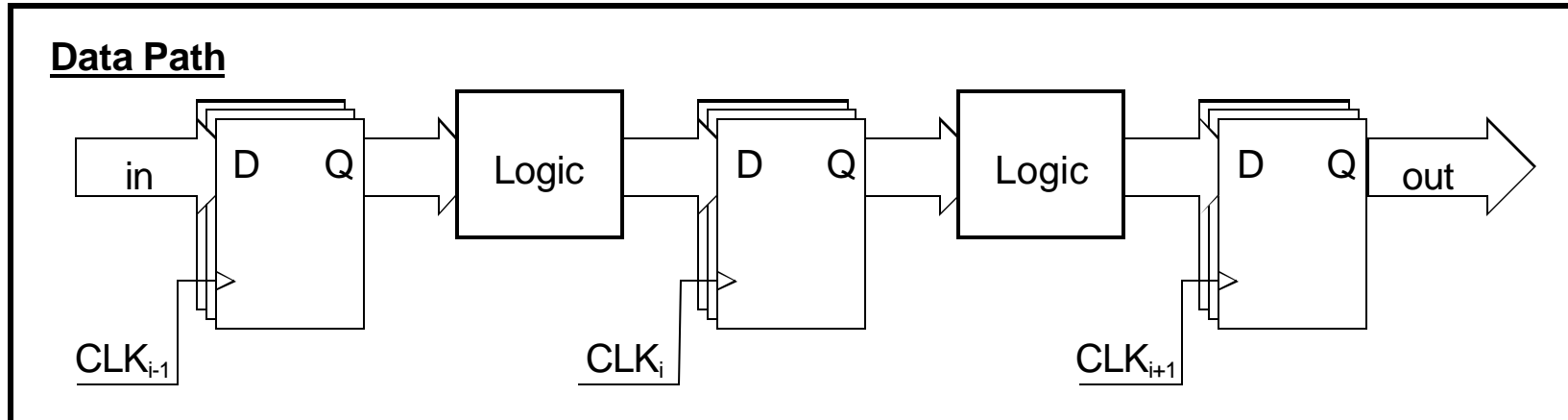


# Clock distribution

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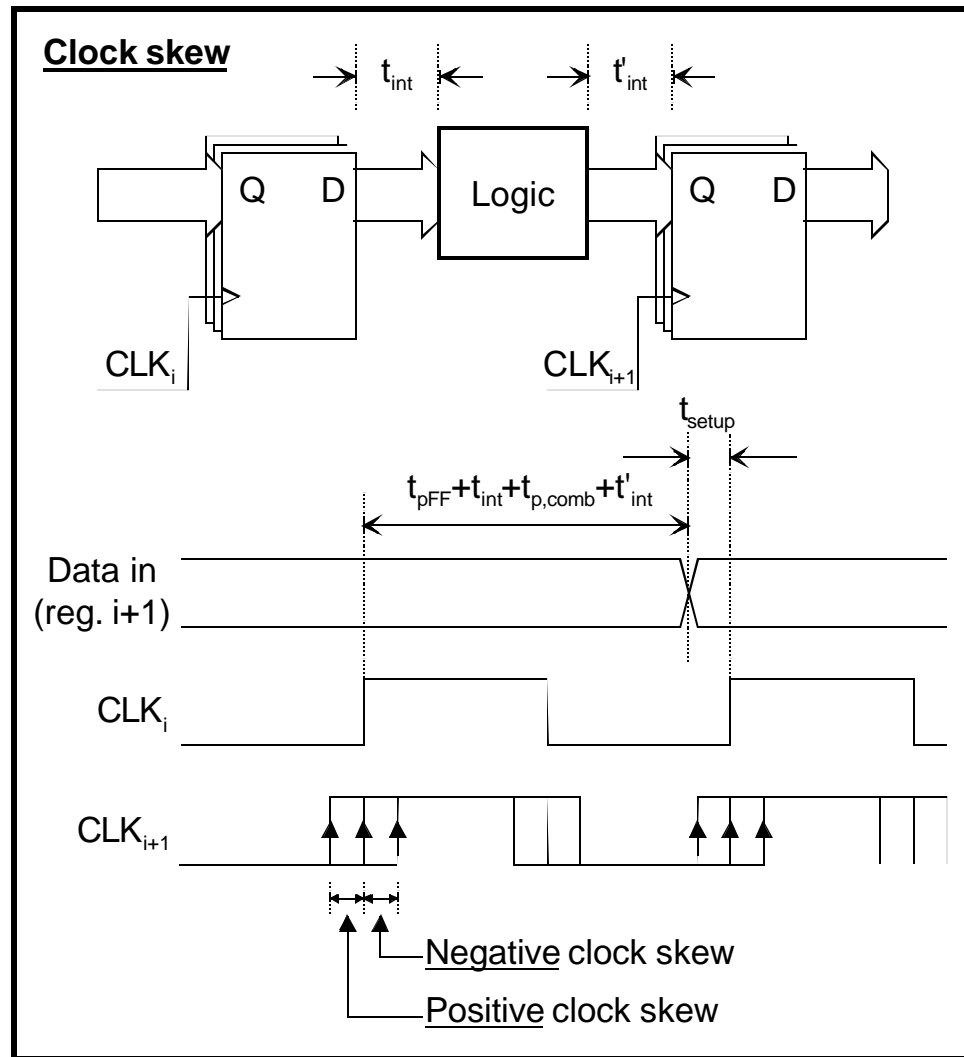
- Clock signals are “special signals”
- Every data movement in a synchronous system is referenced to the clock signal
- Clock signals:
  - Are typically loaded with high fanout
  - Travel over the longest distances in the IC
  - Operate at the highest frequencies

# Clock distribution



- “Equipotential” clocking:
  - In a synchronous system all clock signals are derived from a single clock source (“clock reference”)
  - Ideally: clocking events should occur at all registers simultaneously ... =  $t(\text{clk}_{i-1}) = t(\text{clk}_i) = t(\text{clk}_{i+1}) = \dots$
  - In practice: clocking events will occur at slightly different instants among the different registers in the data path

# Clock distribution



# Clock distribution

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- Skew: difference between the clocking instants of two “sequential” registers:

$$\text{Skew} = t(\text{CLK}_i) - t(\text{CLK}_{i+1})$$

- Maximum operation frequency:

$$T_{\min} = \frac{1}{f_{\max}} = t_{dFF} + t_{\text{int}} + t_{p,\text{comb}} + t'_{\text{int}} + t_{\text{setup}} + t_{\text{skew}}$$

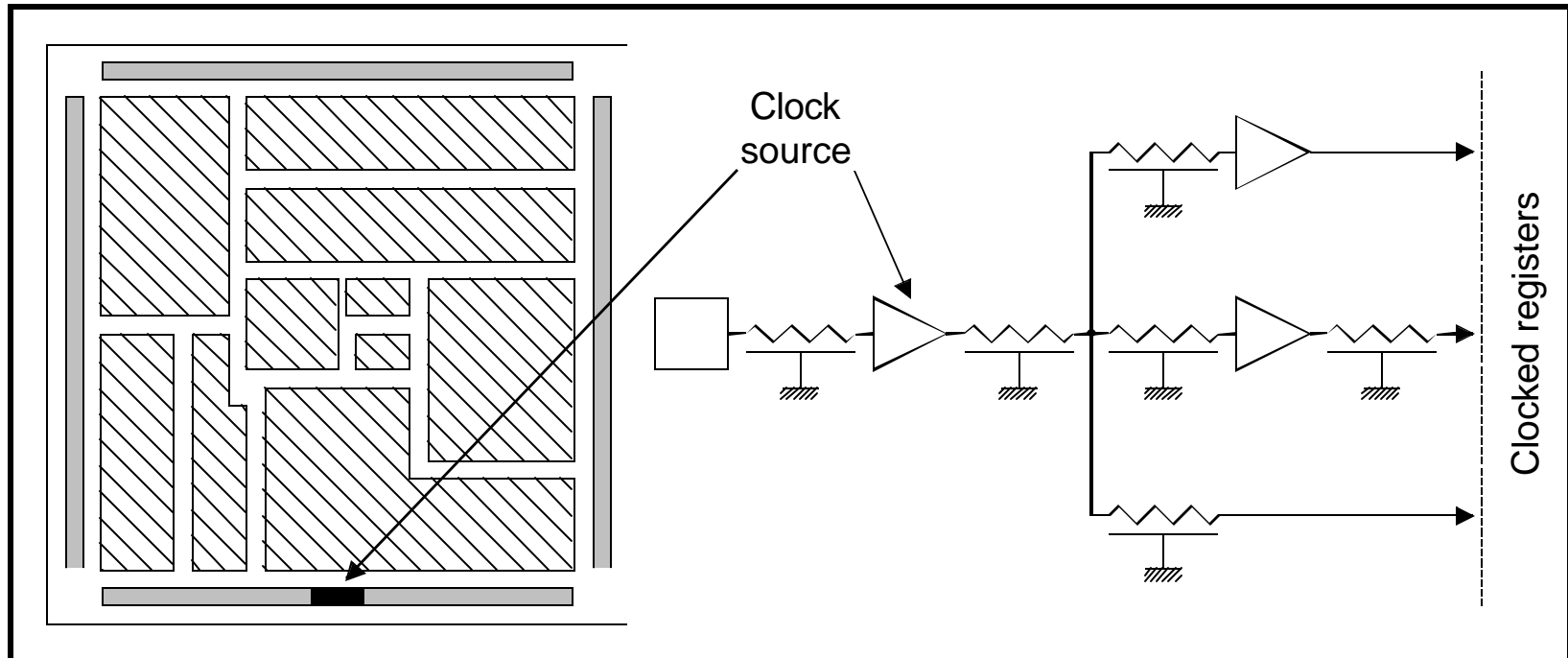
- Skew > 0, decreases the operation frequency
- Skew < 0, can be used to compensate a critical data path BUT this results in more positive skew for the next data path!

# Clock distribution

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- Different clock paths can have different delays due to:
  - Differences in line lengths from clock source to the clocked registers
  - Differences in delays in the active buffers within the clock distribution network:
    - Differences in passive interconnect parameters (line resistance/capacitance, line dimensions, ...)
    - Differences in active device parameters (threshold voltages, channel mobility)
- In a well designed and balanced clock distribution network, the distributed clock buffers are the principal source of clock skew

# Clock distribution



- **Clock buffers:**
  - Amplify the clock signal degraded by the interconnect impedance
  - Isolate the local clock lines from upstream load impedances

# Clock distribution

