ANALOGUE CIRCUITS

TECHNIQUES

Part I

April 16th , 2002

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Outline

From “active” components available in modern IC technologies, to the examples of amplifiers design used for High Energy Physics applications

- 1- Introduction to analogue circuit
- 2- Active elements in Integrated Circuit
- 3- The bipolar transistor

Outline

- 4- Basic of amplifier
- 5- Differential amplifier
- 6- OTA
- 7- Two-stage differential amplifier
- 8- Other amplifiers circuits
- 9- Cascode circuits

- 10- Charge Preamplifier
- 11- Transimpedance Preamplifier
- 12- Preamplifiers conclusions

1- Introduction to analogue circuit

We will NOT talk about :

- A lot of different circuit configurations used for applications in HEP, or outside of HEP (broadband telecommunications, HF, audio, etc …)

- A lot of parameters which may widely influence a final circuit design (like DC operating point, offsets, internal noise sources, sensitivities to external sources, components non-uniformities, etc …)

We will MAINLY talk about :

- Some major aspects of linear amplifier design : building blocks, amplifier stability, amplifier gain, signal bandwidth

- Two examples of signal amplifiers circuits developed for detector front-end

1- Introduction to analogue circuit

REFERENCES:

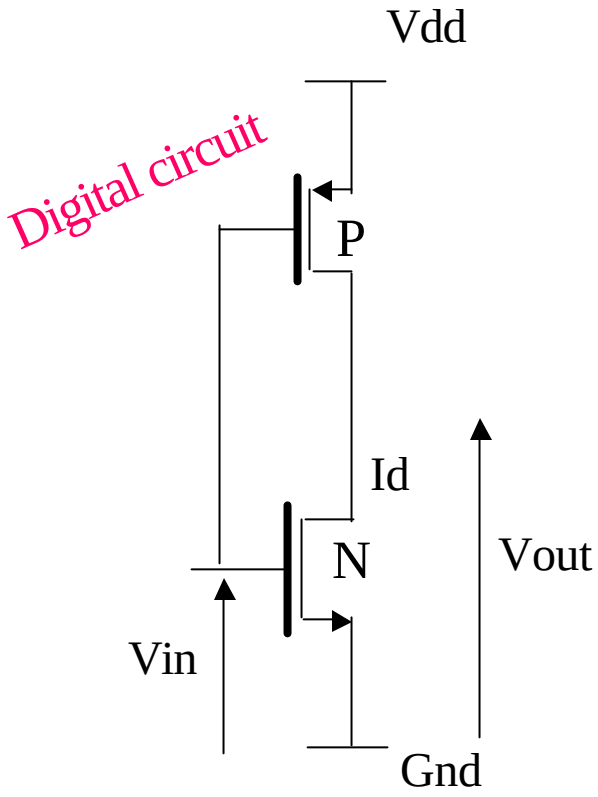
books

IC technology	“Physics in Semiconductor Devices” S. M. Sze, Wiley
Amplifier design	“Analog Integrated Circuits” Paul. R. Gray, Robert. G. Meyer, Wiley
Detector Amplifier design	“Low-Noise Wide-band Amplifiers in Bipolar and CMOS technologies” Z. Y. Chang, Willy M.C. Sansen, Kluwer Academic Publishers

http

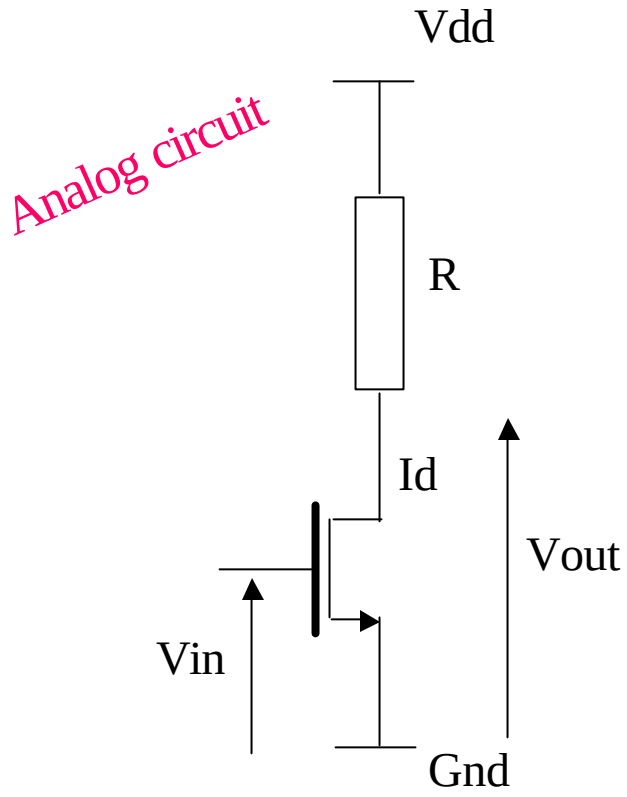
http://www.prenhall.com/howe3/microelectronics/

1- Introduction to analogue circuit



Vin=Gnd (0) or Vdd (1)
Vout = Vdd(1) or Gnd(0)

NON LINEAR SYSTEM

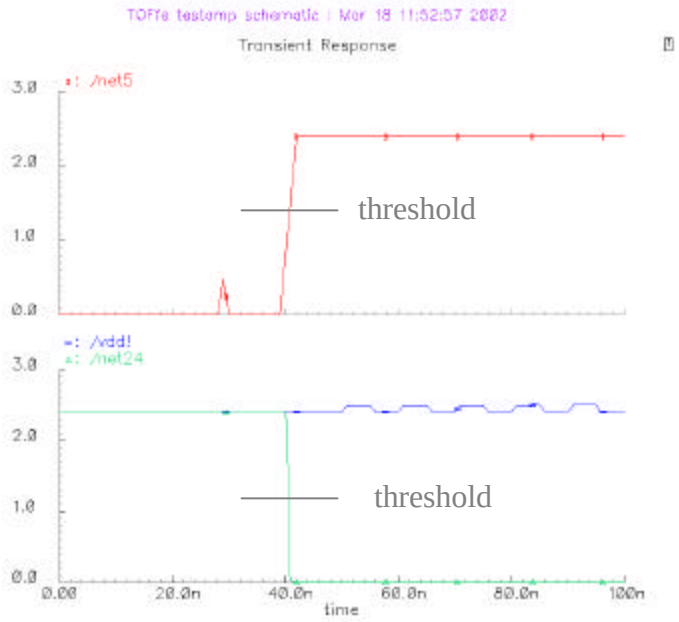


Vout=f(Vin)
Vin and Vout can take any value between Vdd and Gnd

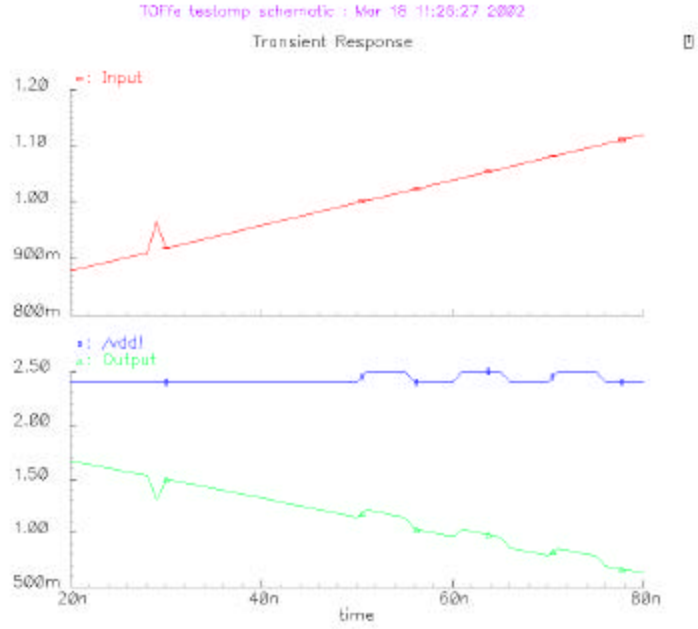
LINEAR SYSTEM

1- Introduction to analogue circuit

Digital circuit



Analog circuit

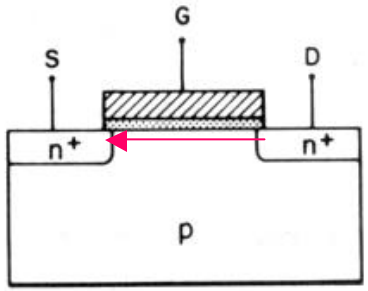


* = up to certain limits !

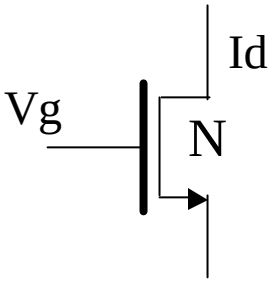
** = function of max. signal range versus noise level

2- Active Components in Integrated Circuit

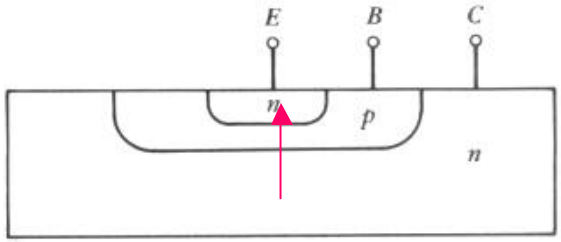
MOS TRANSISTOR



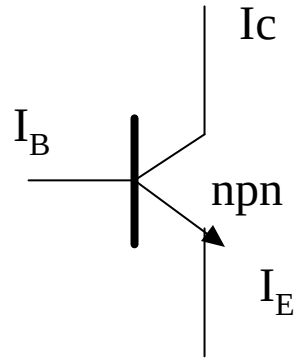
Surface effect conduction under the control of the gate potential



BIPOLAR TRANSISTOR

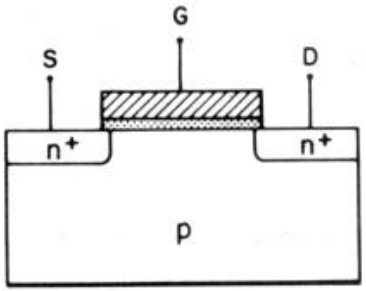


Volume effect conduction under the control of the junctions potential



2- Active Components in Integrated Circuit

MOS TRANSISTOR



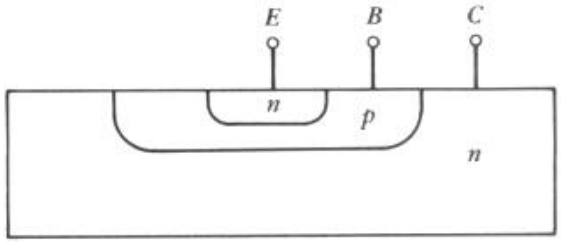
$$I_d = K_0 . \frac{W}{L} . (Vgs - Vt)^2$$

W/L=transistor aspect ratio

Ko=f(mobility, gate capacitance, T, …)

Vt=f(dopant, gate capacitance, fixed charges, …)

BIPOLAR TRANSISTOR

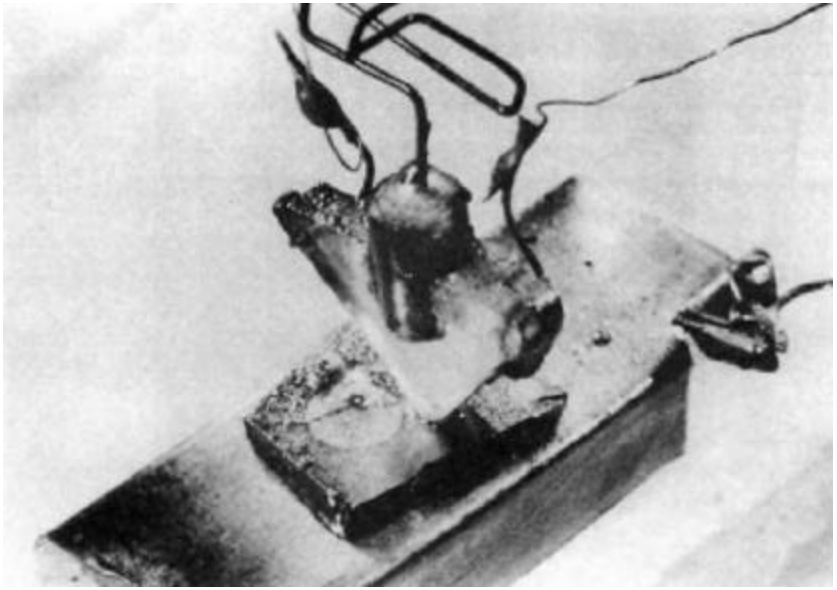


$$Ic = Is . \exp V_{BE} / U_T$$

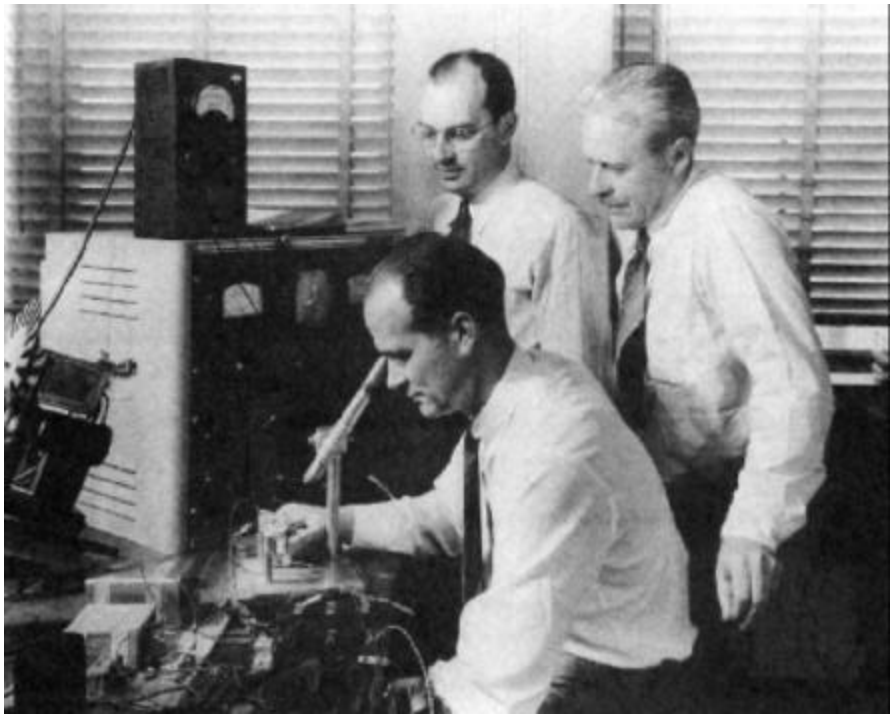
$$U_T = \frac{k \cdot T}{q}$$

Only “fundamental” quantities
(k= Boltzman constant, T= Temp., q= electron charge)

3- The Bipolar Transistor



FIRST SOLID STATE TRANSISTOR (1947)



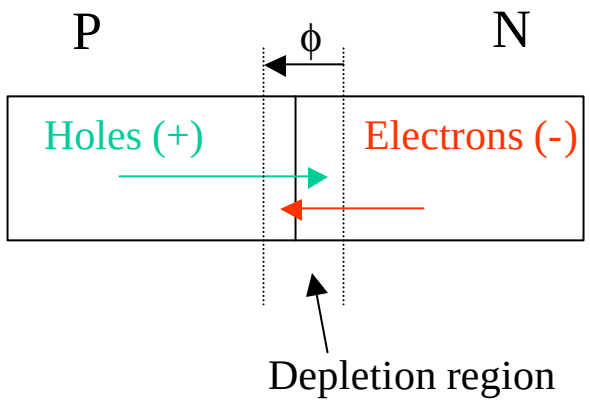
BARDEEN, BRATTAIN AND SHOCKLEY

3- The Bipolar Transistor

p-n junction

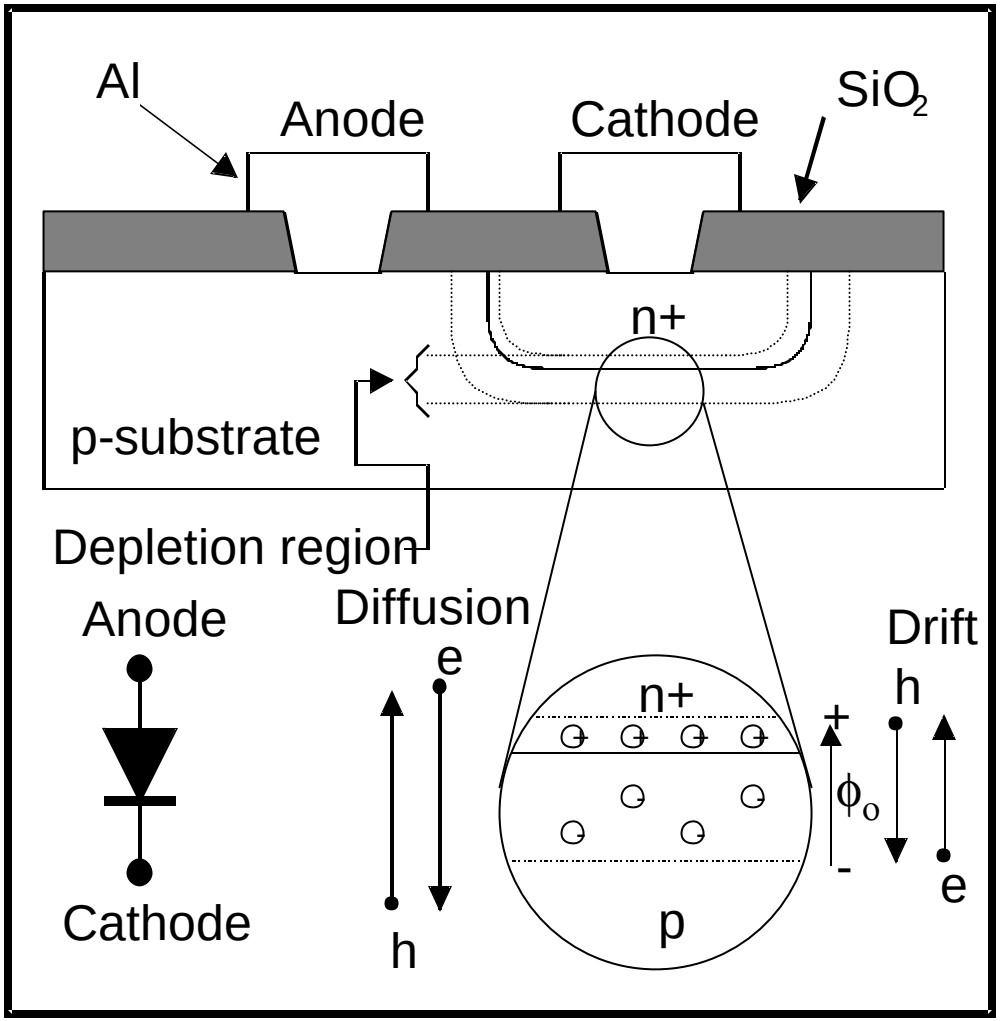
A pn-junction in Silicon is the abutment of two Si volumes with free carriers of opposite polarities

- Majority carriers diffuse from regions of high to regions of low concentration
- An electric potential is created, which counteracts the diffusion current (drift current)
- In equilibrium there is no net flow of carriers in the diode



3- The Bipolar Transistor

p-n junction



3- The Bipolar Transistor

p-n junction

- Under zero bias there is a built-in potential across the junction
- The built-in potential is:

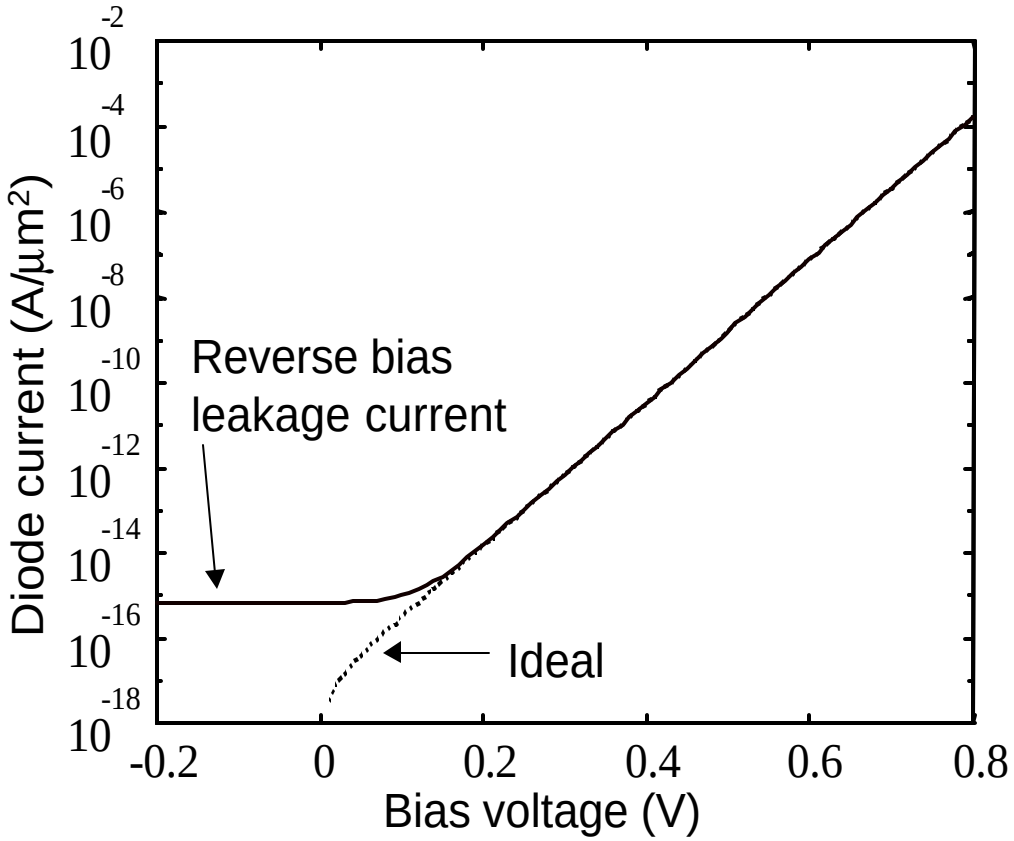
$$f_0 = U_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$$

$$U_T = \frac{k \cdot T}{q} \cong 26\,\text{mV} \;@\; 300°\text{K}$$

$$n_i = 1.5 \times 10^{10}\ \text{cm}^{-3}\ \text{for silicon @}\ 300°\,\text{K}$$

3- The Bipolar Transistor

p-n junction



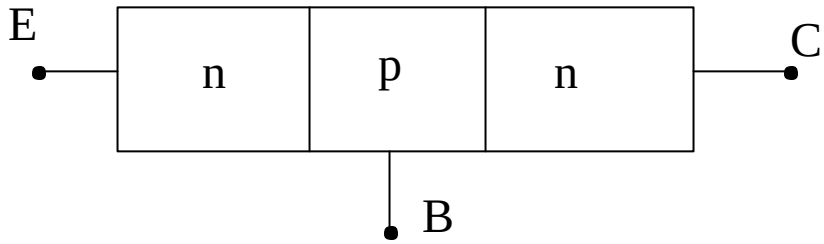
- For $V>\phi_T$ (forward bias)

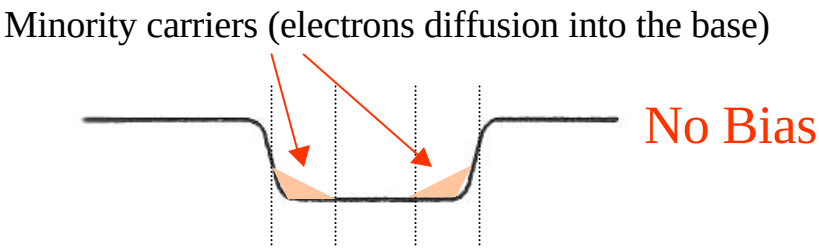
$$I_F \cong I_s \cdot e^{V/U_T}$$

- For $V<0$ (reversed bias)

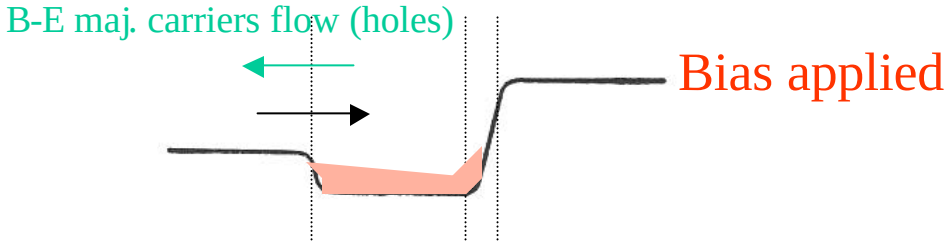
$$I_R \cong -I_s$$

3- The Bipolar Transistor





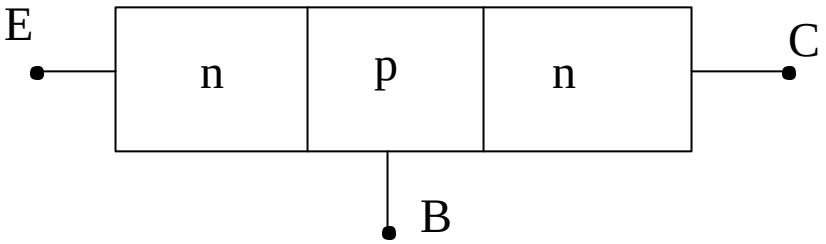
Barrier is lowered : more electrons (min. carriers) diffuse to the base, may reach the opposite junction, and contribute to the current of the reverse_biased BC junction

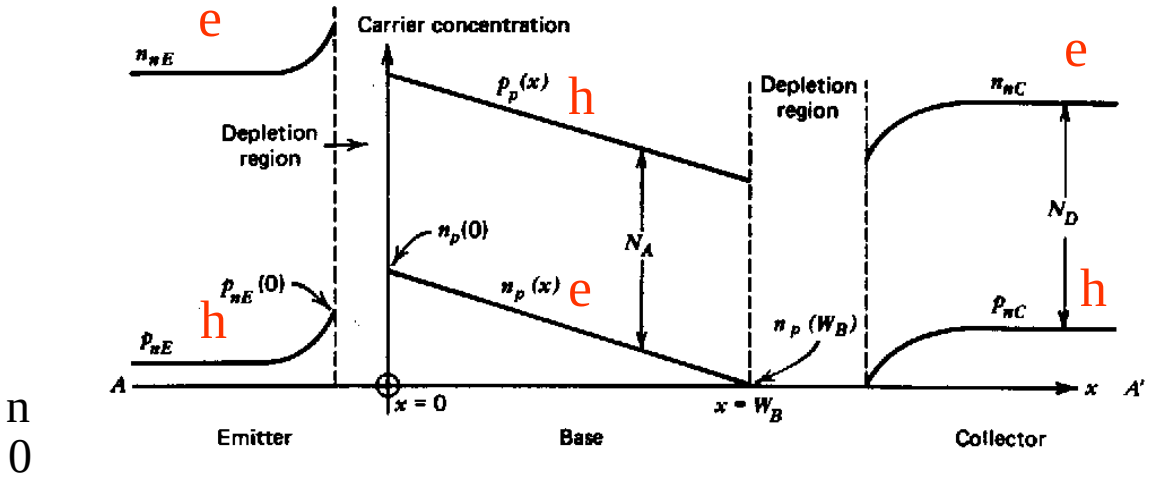


Base-Emitter
Junction is forward biased

Collector-Base
Junction is reverse biased

3- The Bipolar Transistor





n
0

Base-Emitter
Junction is forward biased

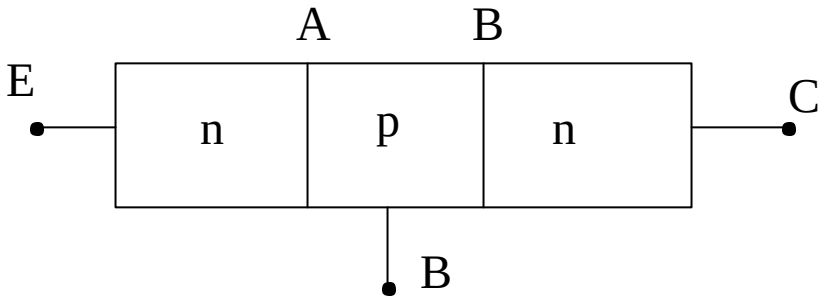
Collector-Base
Junction is reverse biased

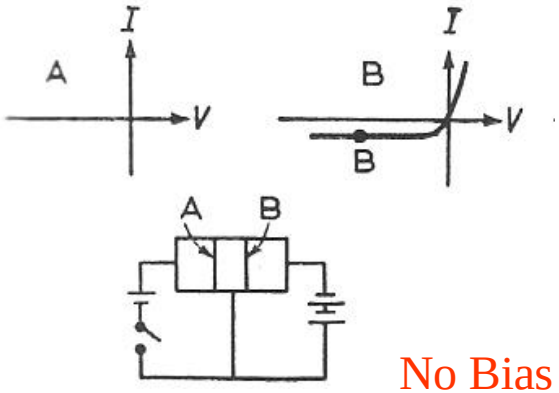
3- The Bipolar Transistor

Conduction mechanism in a bipolar transistor is made of the MINORITY CARRIERS flowing through the base region

Currents are flowing through semiconductors junctions, within the crystalline structure. Not a surface effect.

3- The Bipolar Transistor

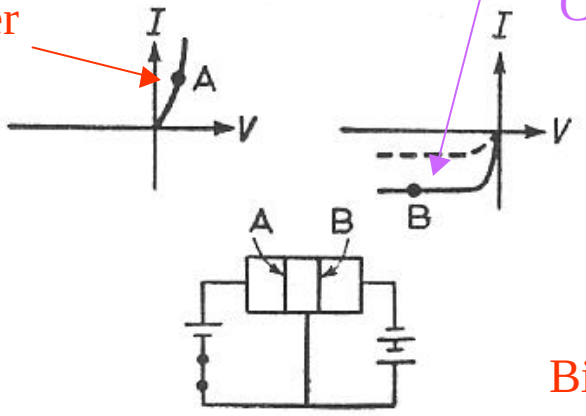




No Bias

Forward biased Base-Emitter Junction

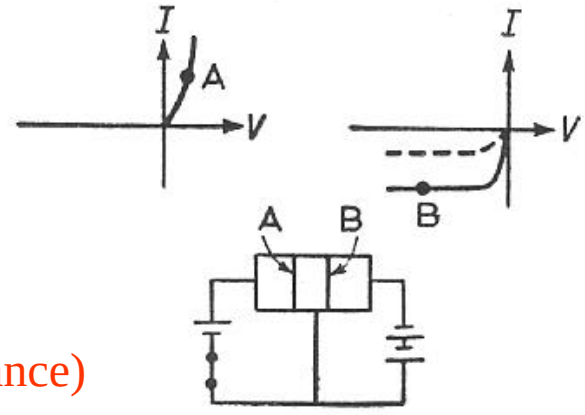
Higher « reverse » current in reverse biased Collector-Base Junction



Bias applied

3- The Bipolar Transistor

Why is bipolar effect an « amplifying » device ?



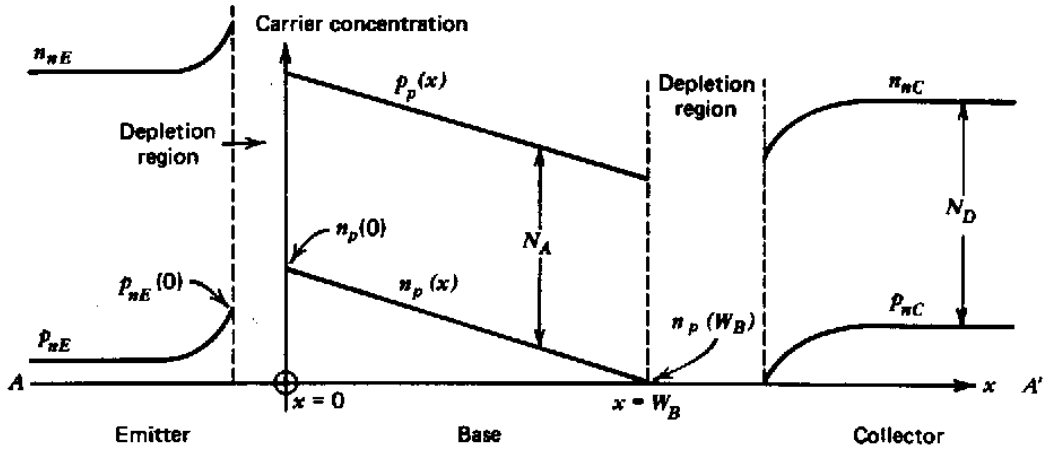
- Currents in junctions A and B are almost equal.
- B-E junction (A) is forward biased (low impedance)
- C-E junction (B) is reverse biased (high impedance)

The collector node being high impedance (current source). It can be loaded with large resistors R_{high}
The output power is $R_{high}.I^2$

The emitter node is low impedance. The power at emitter node is $R_{low}.I^2$

The output power (at collector) is higher than the input power (at emitter)

3- The Bipolar Transistor



Minority carriers concentration at x=0

$$n_p(0) = n_{p0} \exp \frac{V_{BE}}{U_T}$$ (diffusion carrier density equation)

N_{p0} is the intrinsec minority carrier concentration in the base and $U_T = \frac{kT}{q}$

K is the boltzmann constant
q the electron charge
T is temperature

$U_T = \frac{kT}{q}$ = 26mV at 300K

3- The Bipolar Transistor

The collector current is the result of the minority carrier concentration in the base crossing the B-E junction due to the electrial field direction

$$Ic = qAD_n \frac{n_p(0)}{W_B}$$

A is cross section of the emitter
Dn is the diffusion constant for electrons (the minority carriers in NPN device)

With the equation of $n_p(0)$

$$Ic = \frac{qAD_n n_{p0}}{W_B} \exp \frac{V_{BE}}{U_T}$$

n_{p0} is the intrinsec minority carrier concentration in the base

3- The Bipolar Transistor

The base current I_B is the result of two current (holes in case of NPN) contributions (namely diffusion current in emitter and recombination current within the base):

$$I_B = \left(\frac{1}{2} qAW_B \frac{n_{p0}}{t_B} + \frac{qAD_P}{L_P} \frac{n_i^2}{N_D} \right) \exp \frac{V_{BE}}{U_T}$$

Both I_C and I_B depend on the same term : $\exp \frac{V_{BE}}{U_T}$

The ratio Ic/Ib is called « forward current gain » :

$$b = \frac{\frac{qAD_n n_{p0}}{W_B}}{\frac{1}{2} qAW_B \frac{n_{p0}}{t_B} + \frac{qAD_P}{L_P} \frac{n_i^2}{N_D}}$$

3- The Bipolar Transistor

β, the current gain between collector and base :

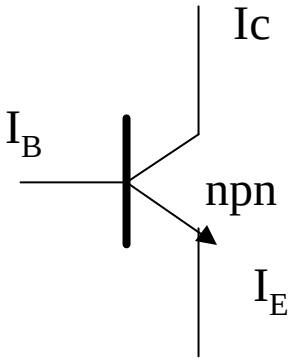
$$b = \frac{1}{\frac{1}{2}\frac{W_B^2}{D_N t_B} + \frac{D_P}{D_N}\frac{W_B}{L_p}\frac{N_A}{N_D}}$$

By maximizing N_A/N_D ratio,and minimizing W_B, the base width, it is possible to reach values of β=50-200

$$Ic = Is.\exp V_{BE}/U_T$$

$$Ic = bI_B$$

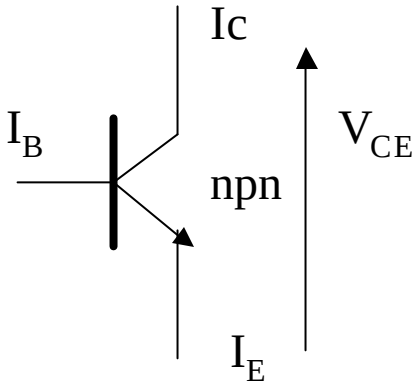
$$I_E = Ic + I_B = (b+1)I_B$$

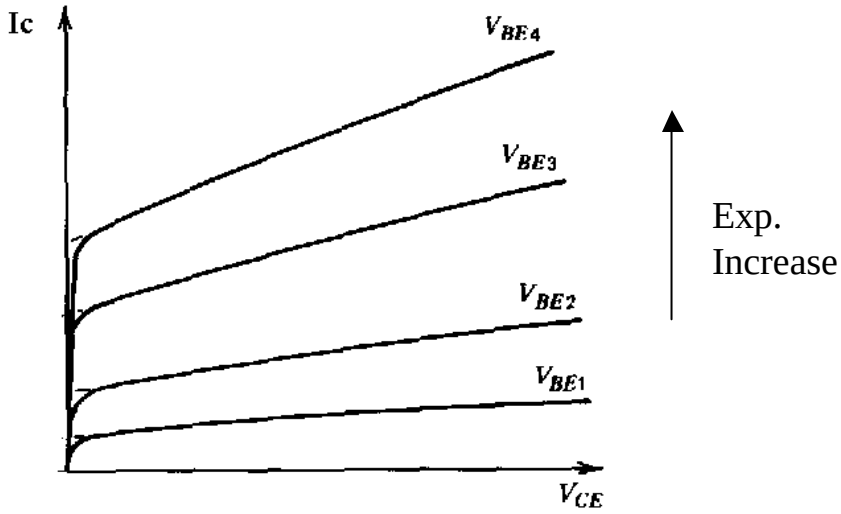


Transconductance :

$$\frac{\Delta Ic}{\Delta V_{BE}} = Ic/U_T$$

3- The Bipolar Transistor



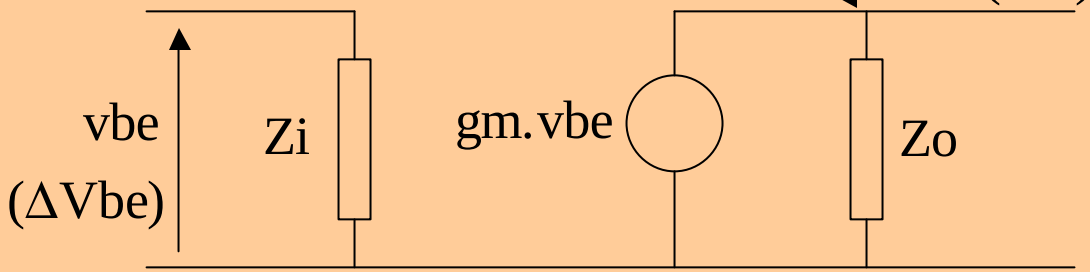


Ic vs. V_{CE} Characterisitc

$$Ic = Is.\exp V_{BE} / U_T$$

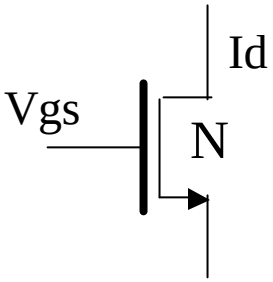
$$\mathrm{gm} = \frac{\Delta Ic}{\Delta V_{BE}} = Ic / U_T$$

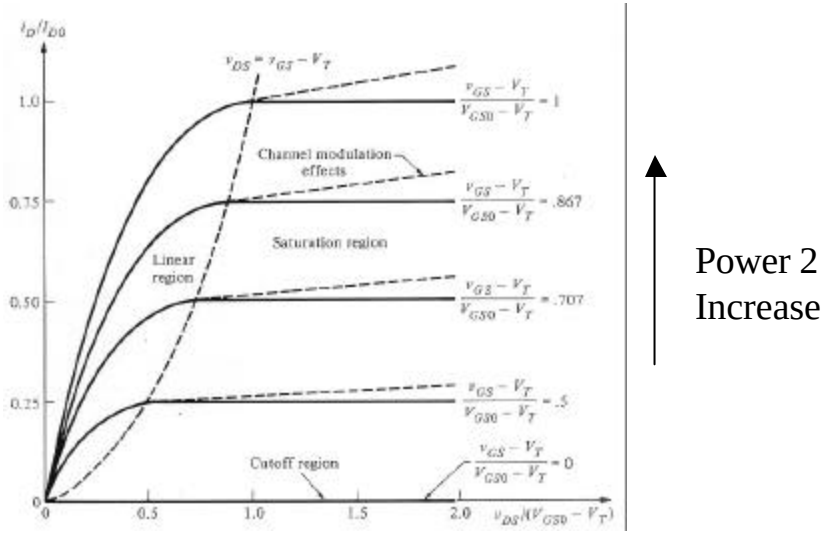
Small signal model



(note : in all transparencies, explicit "-" sign is ignored)

Reminder : The MOS Transistor



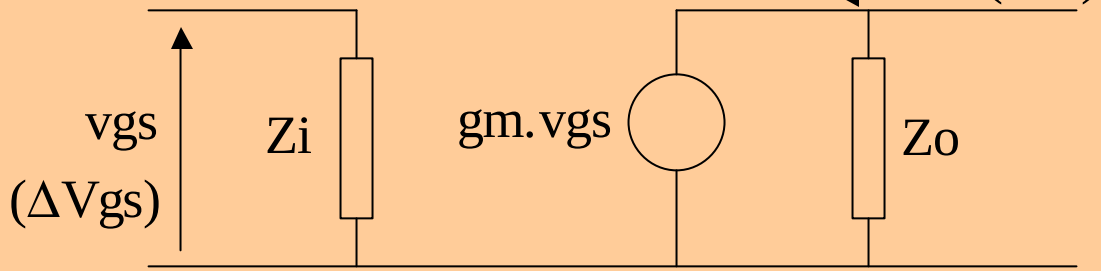


Id vs. V_{ds} Characteristics

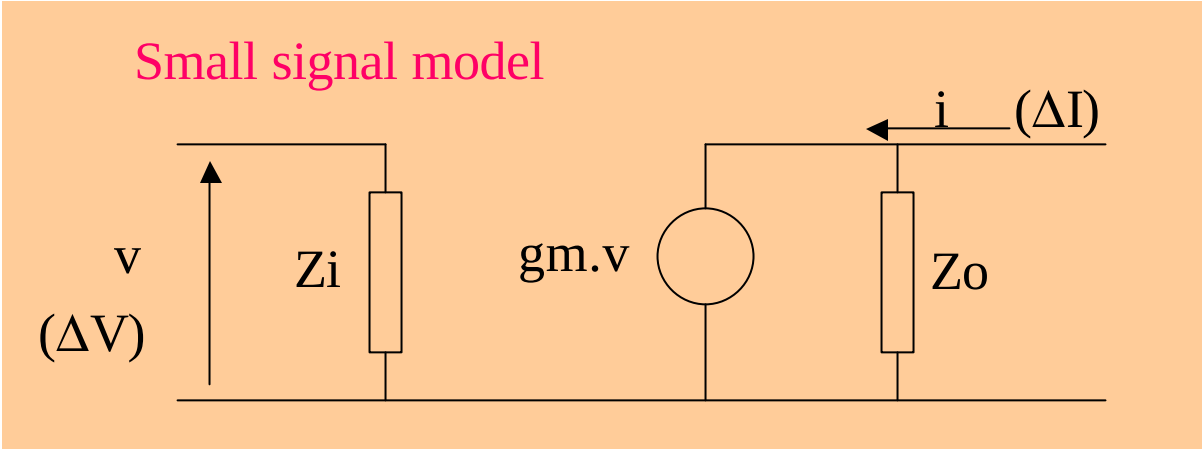
$$I_d = K_0 . \frac{W}{L} . (Vgs - Vt)^2$$

$$\mathrm{gm} = \frac{\Delta I_d}{\Delta Vgs} = 2\sqrt{K_o . \frac{W}{L} . I_d}$$

Small signal model



Linear models for Bipolar or MOS Transistor



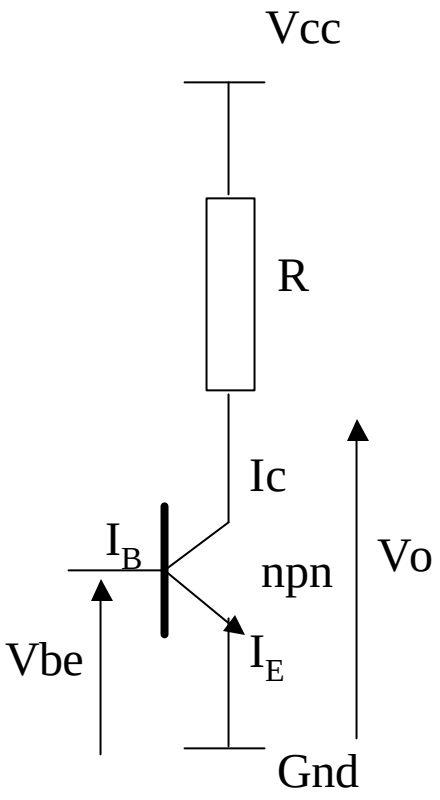
For most linear applications, both MOS or bipolar are represented by similar model elements

Values inside the model are different :

	Bipolar	MOS
Zi	Low R	High C
Zo	High R	High R
gm	Max.	Process dependent

4- Basic of amplifier

The simplest amplification circuit



$$V_o = Vcc - R.I_c$$

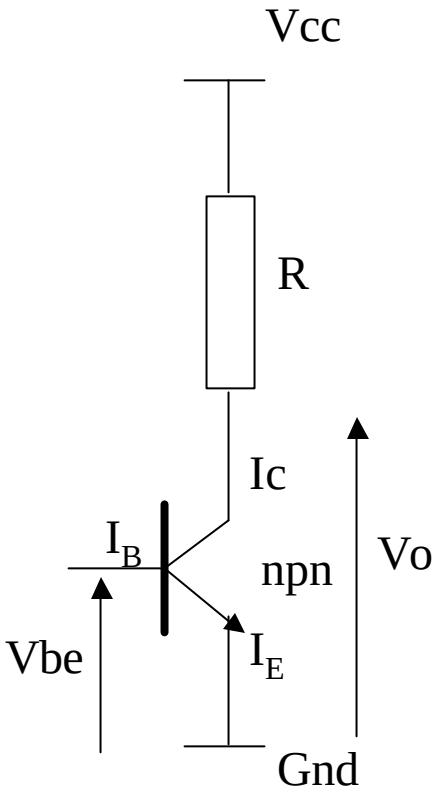
$$I_c = I_s.e^{Vbe/Ut}$$

The collector of the npn transistor behaves as a current source : delivery of current “Ic” from a high impedance node

The voltage gain is given by Vo variation vs. Vbe variation

4 - Basic of amplifier

The voltage gain is given by Vo variation vs. Vbe variation



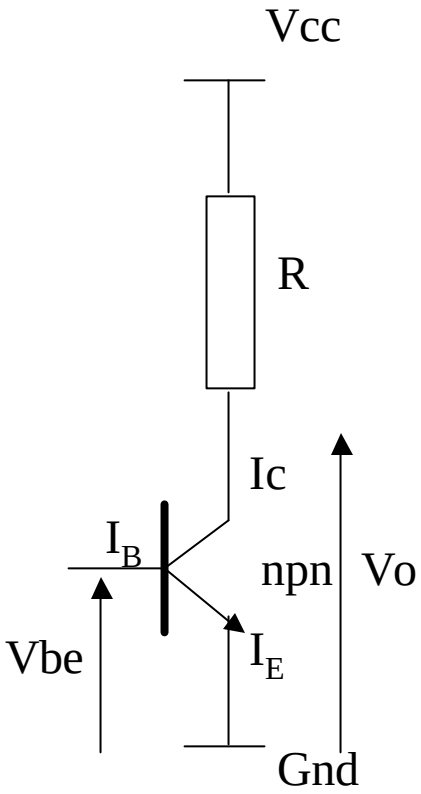
$$V_o = Vcc - R.I_c \Rightarrow \Delta V_o = R.\Delta I_c$$

$$I_c = I_s.e^{Vbe/Ut}$$

$$\frac{\Delta I_c}{\Delta Vbe} = \frac{1}{Ut}.I_s.e^{Vbe/Ut} = \frac{I_c}{Ut}$$

4 - Basic of amplifier

The voltage gain is given by Vo variation vs. Vbe variation



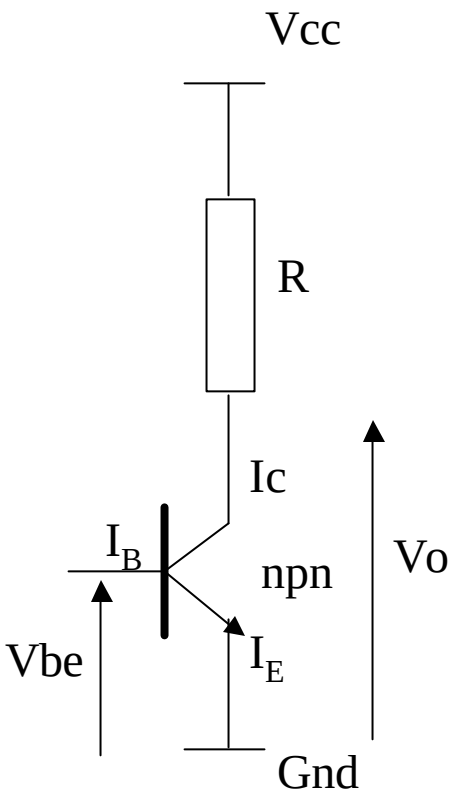
$$\frac{\Delta V_o}{\Delta Vbe} = R.\frac{I_c}{Ut}$$

$$\frac{\Delta I_c}{\Delta Vbe} = \frac{I_c}{Ut}$$

Is called the transconductance ‘gm’

$$\frac{\Delta V_o}{\Delta Vbe} = \mathrm{R.gm}$$

4 - Basic of amplifier



$$\frac{\Delta V_o}{\Delta Vbe} = \mathrm{R.gm} \qquad \mathrm{gm} = \frac{I_c}{Ut}$$

Typical values :

$$Ut = {kT}/{q} = 26mV\ @\ 25de.C$$

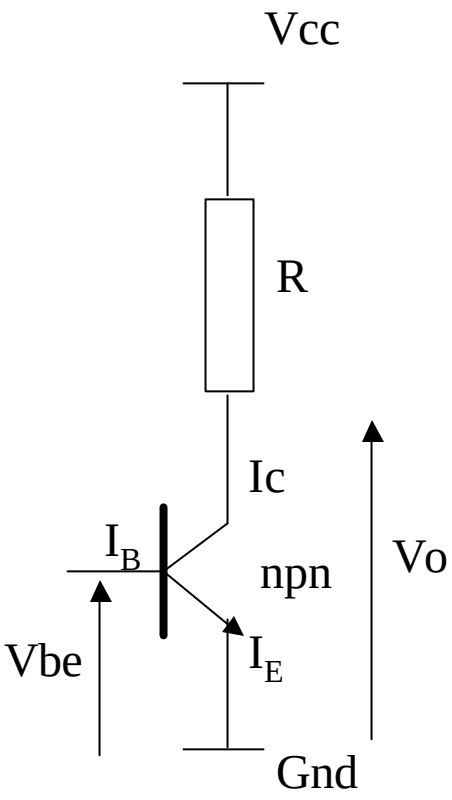
$$Ic = 1mA$$

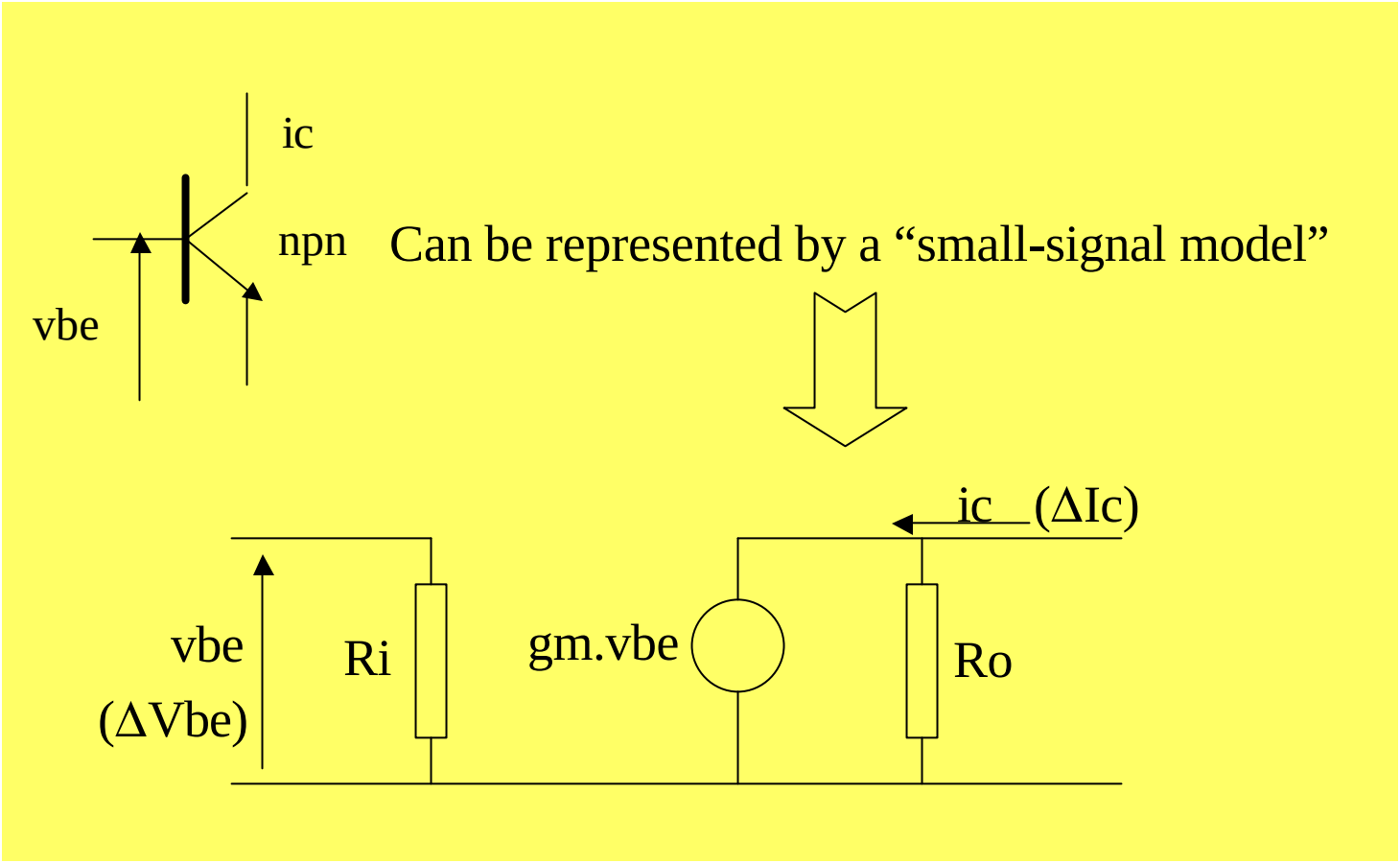
$$R = 1Kohms$$

$$\mathrm{gm} = 38.5mS$$

$$\frac{\Delta V_o}{\Delta Vbe} = 38.5$$

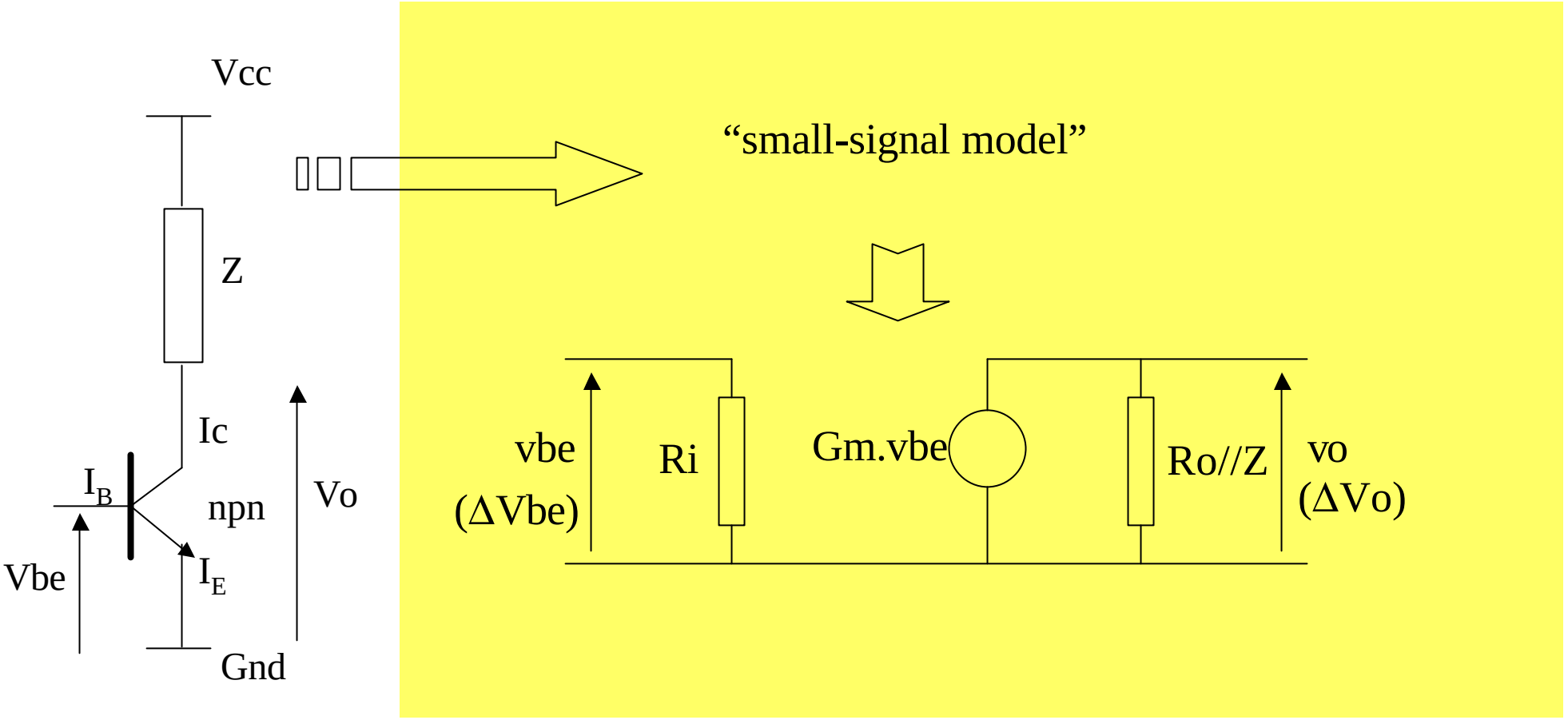
4 - Basic of amplifier





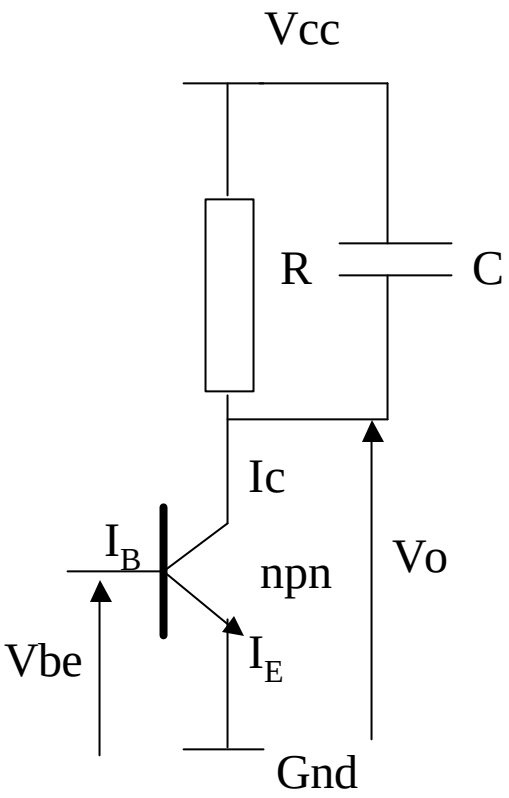
Ri, Ro represent the input and output impedances of the non-ideal transistor

4 - Basic of amplifier

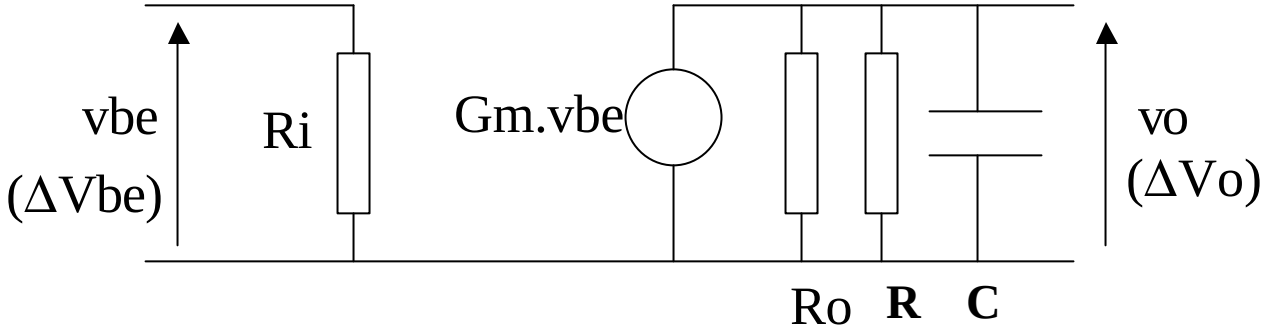


Ri, Ro represent the input and output impedances of the non-ideal transistor

4 - Basic of amplifier



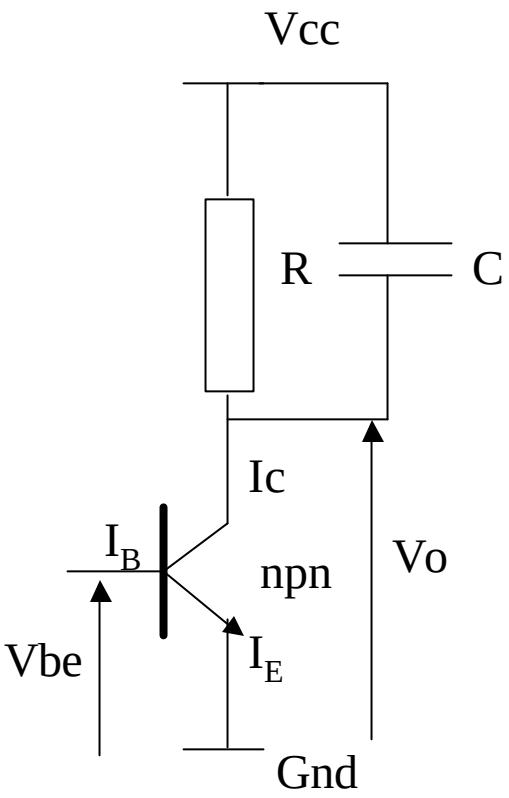
A very simple Gain-Bandwidth calculation model



Usually Ro (output impedance of transistor) is much higher than R. The output stage has one single pole created by the resistive load (which defines gain) and the capacitive load.

$$\frac{v_0}{v_i} = gm \,.\, \left(\frac{R.\frac{1}{sC}}{R + \frac{1}{sC}} \right)$$

4 - Basic of amplifier



$$\frac{v_0}{v_i} = gm \,.\, R.\left(\frac{1}{1+sRC}\right)$$

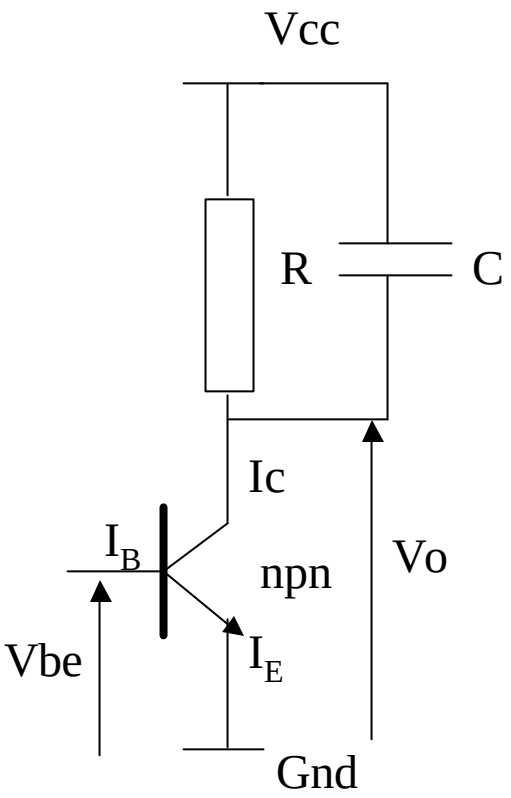
The circuit gain at low frequency is : gm.R (as expected)

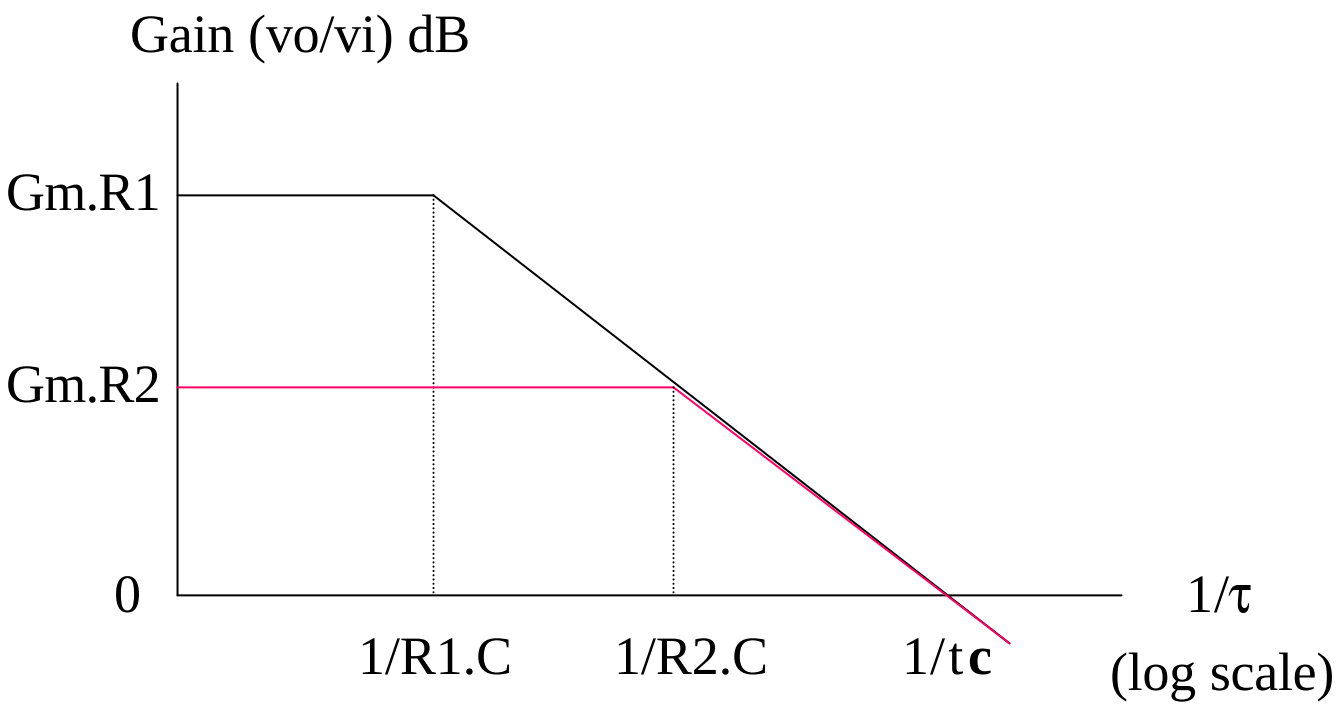
The circuit transfer function has one pole at t =RC

The circuit bandwidth limit (Gain >1) is at :

$$t_c = gm^{-1} \,.\, C$$

4 - Basic of amplifier



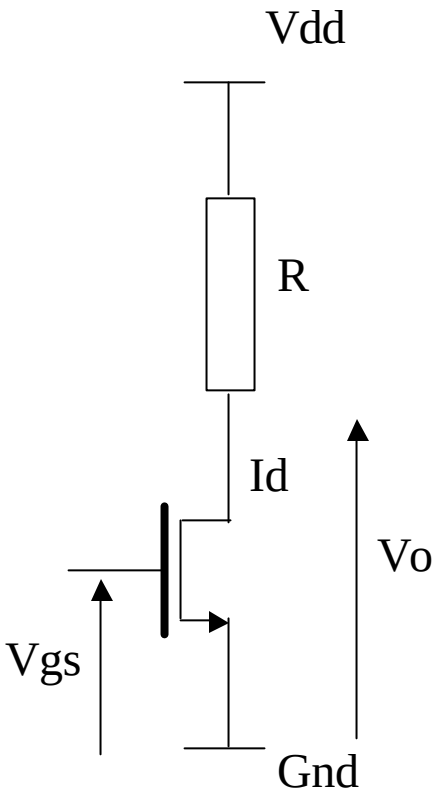


$$t_c = gm^{-1}.C$$

The maximum bandwidth of gain circuit with one pole is given by the input device transconductance and capacitive load.

Example : gm = 10^{-2}, C=1pF, τc=100ps, fc=1.6GHz

4 - Basic of amplifier



The simplest amplification circuit with a MOS transistor instead of a bipolar one.

$$V_o = V_{dd} - R.I_d$$

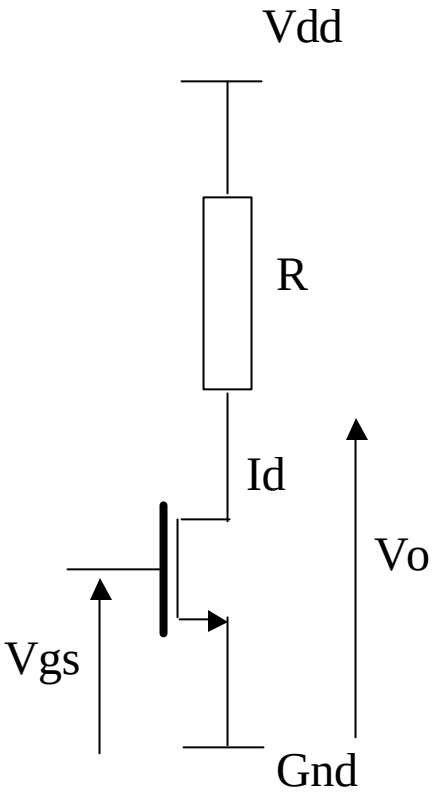
$$I_d = K_0 . \frac{W}{L} . (Vgs - Vt)^2$$

The drain of the MOS transistor behaves as a current source : delivery of current “Id” from a high impedance node

The voltage gain is given by Vo variation vs. Vgs variation

4 - Basic of amplifier

The voltage gain is given by Vo variation vs. Vgs variation



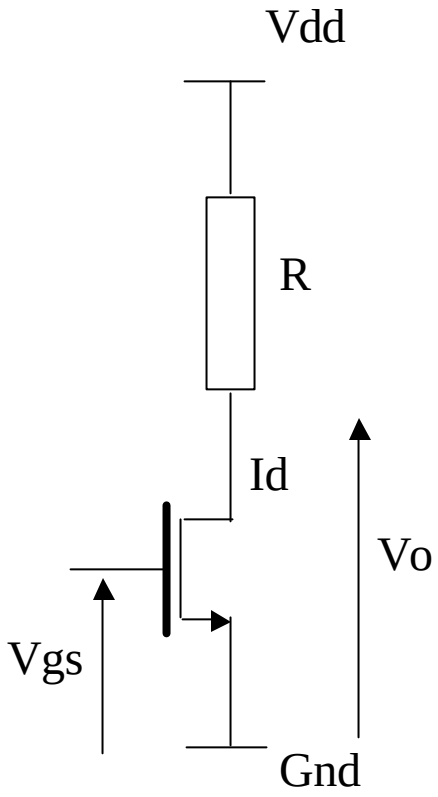
$$\Delta V_o = R.\Delta I_d$$

$$I_d = K_0.\frac{W}{L}.(Vgs - Vt)^2$$

"gm" transconductance of MOS device

$$\Delta I_d = 2\sqrt{K_o.\frac{W}{L}.I_d}.\Delta Vgs$$

4 - Basic of amplifier

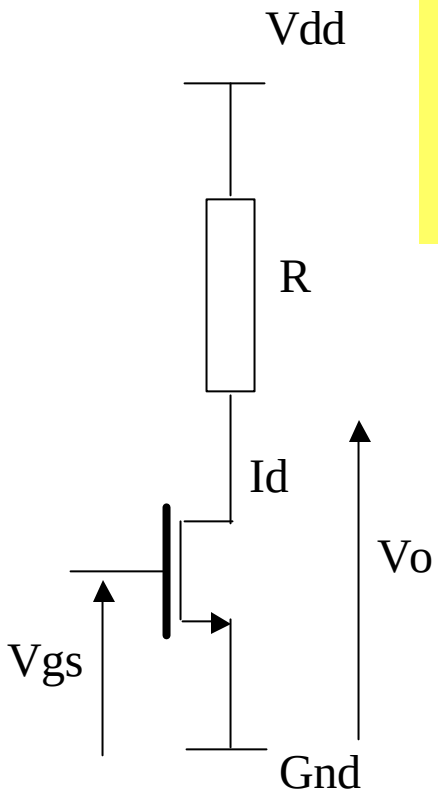


$$gm = 2\sqrt{K_o . \frac{W}{L} . I_d}$$

The voltage gain is given by Vo variation vs. Vgs variation

$$\frac{\Delta V_o}{\Delta Vgs} = R.gm$$

4 - Basic of amplifier



$$\frac{\Delta V_o}{\Delta Vgs} = \mathrm{R.gm} \qquad \frac{\Delta I_d}{\Delta Vgs} = 2\sqrt{K_o . \frac{W}{L} . I_d}$$

Typical values for modern MOS technology:

$$K_0 = 150.10^{-6}\, A/V^2 \qquad \frac{W}{L} = 100$$

$$Id = 1mA$$

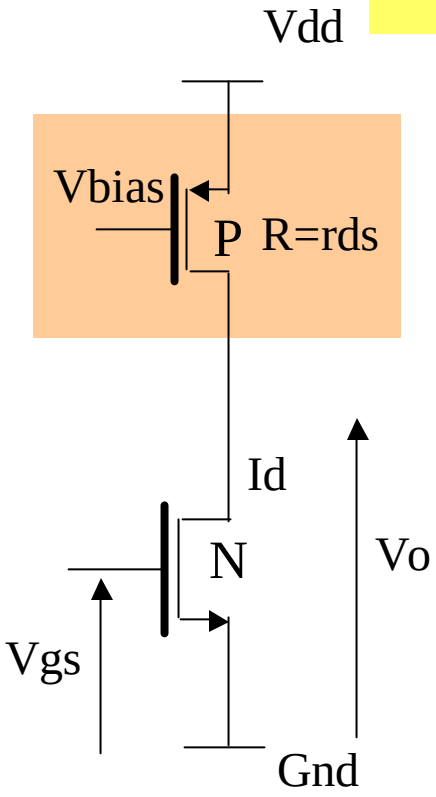
$$R = 1Kohms$$

$$\mathrm{gm} = 7.8mS$$

$$\frac{\Delta V_o}{\Delta Vgs} = 7.8$$

4 - Basic of amplifier

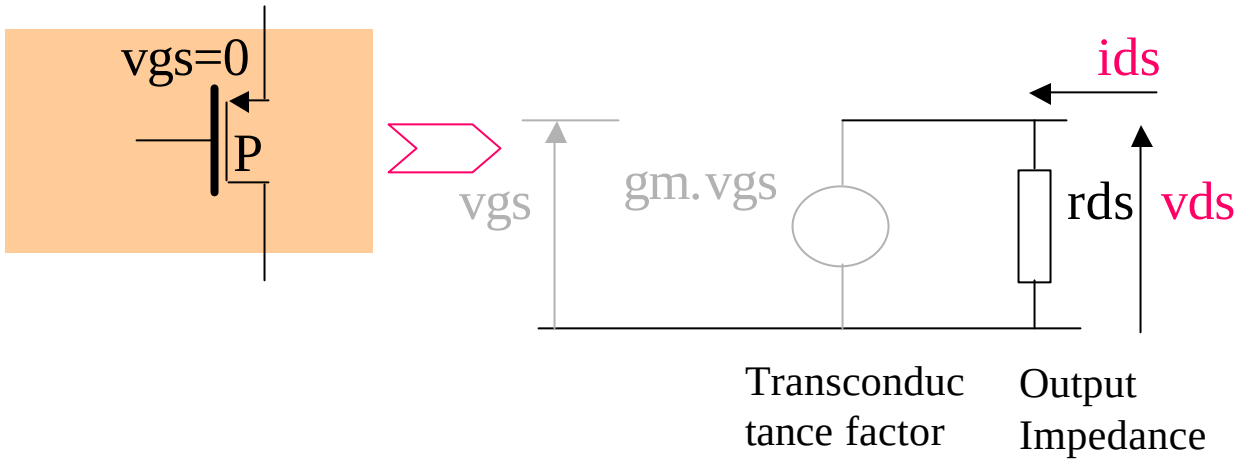
VARIANT WITH “ACTIVE LOAD”



The resistor load can be replaced by a transistor working as a current source.

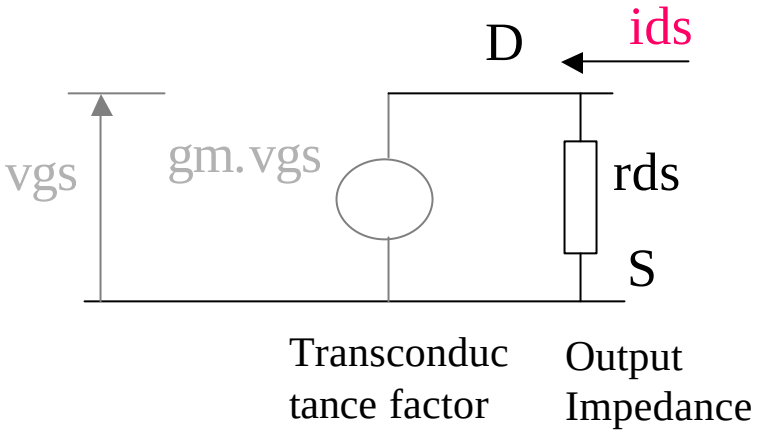
The high output impedance (drain of PMOS) is used as the load.

Small signal model

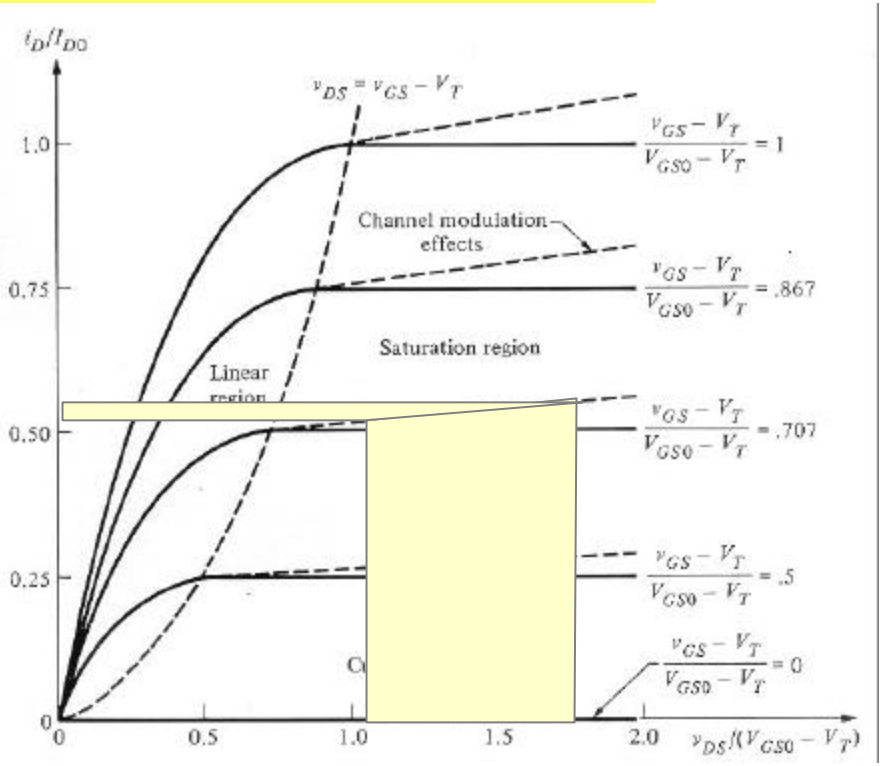


4 - Basic of amplifier

VARIANT WITH “ACTIVE LOAD”



Ids

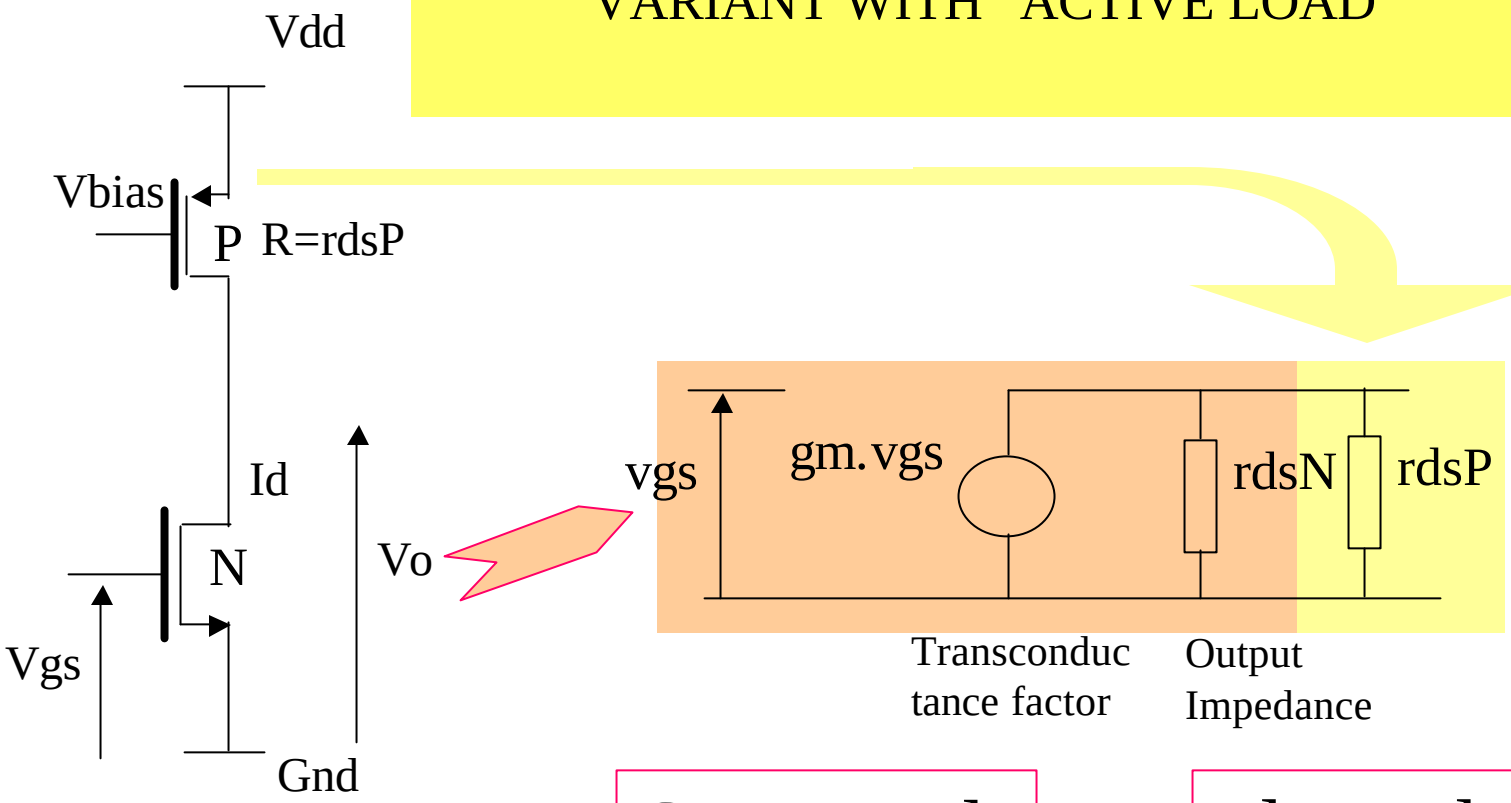


Vds

Δids/Δvds is small -→ Equivalent output resistance is high
(usually 50K to 1Mohms)

4 - Basic of amplifier

VARIANT WITH “ACTIVE LOAD”

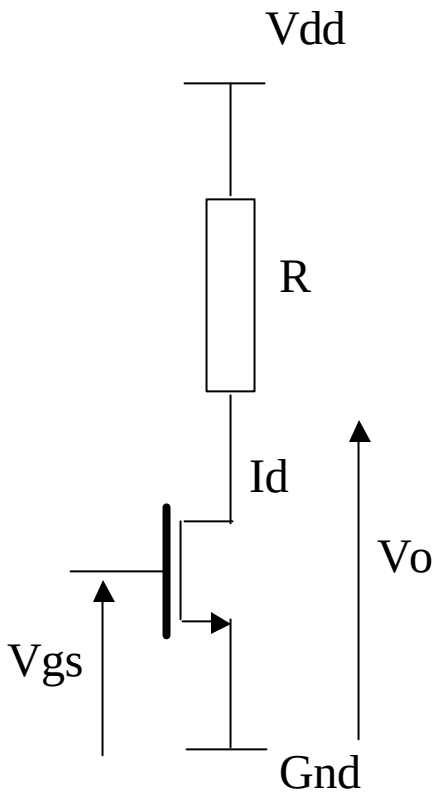


$G = gm.rds$ and $rds = rdsN//rdsP$

rds is usually large (>50K-1M ohms). Gain G reaches ~100 (40dB)

4 - Basic of amplifier

SINGLE-ENDED STRUCTURE

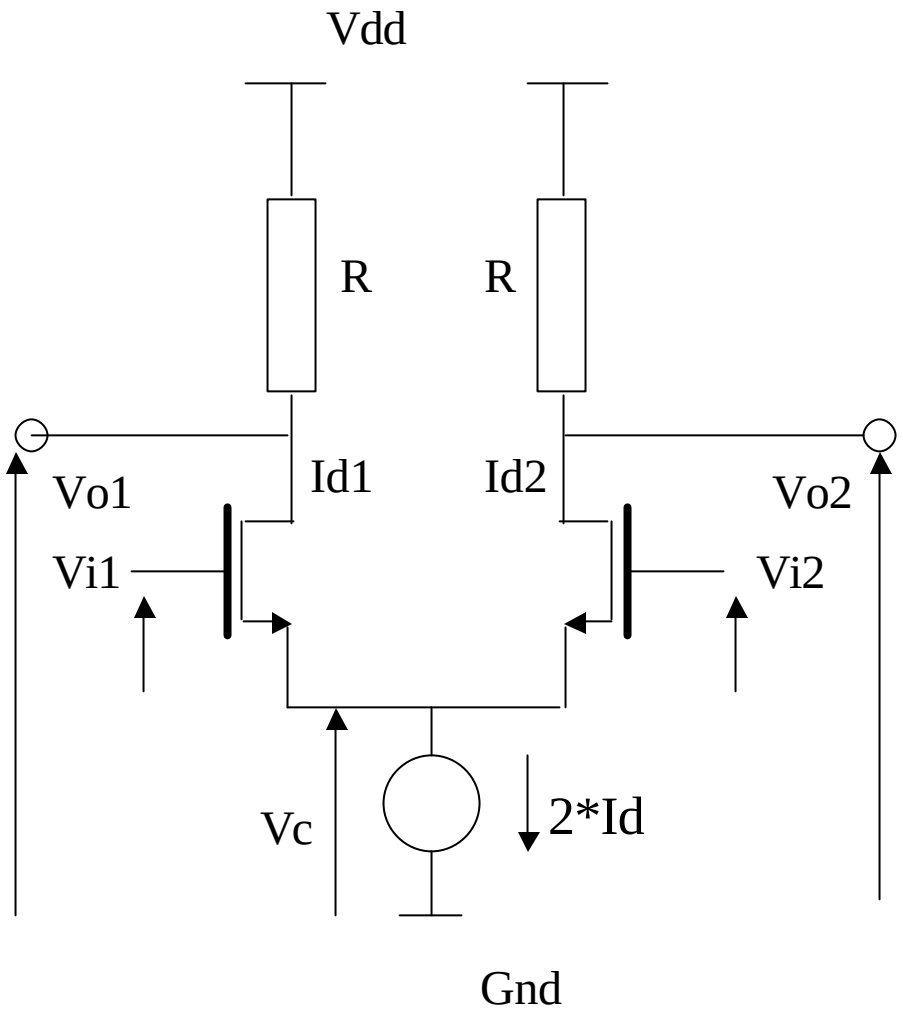


• Output is sensitive to Vdd/Gnd fluctuation (poor Power Supply Rejection)

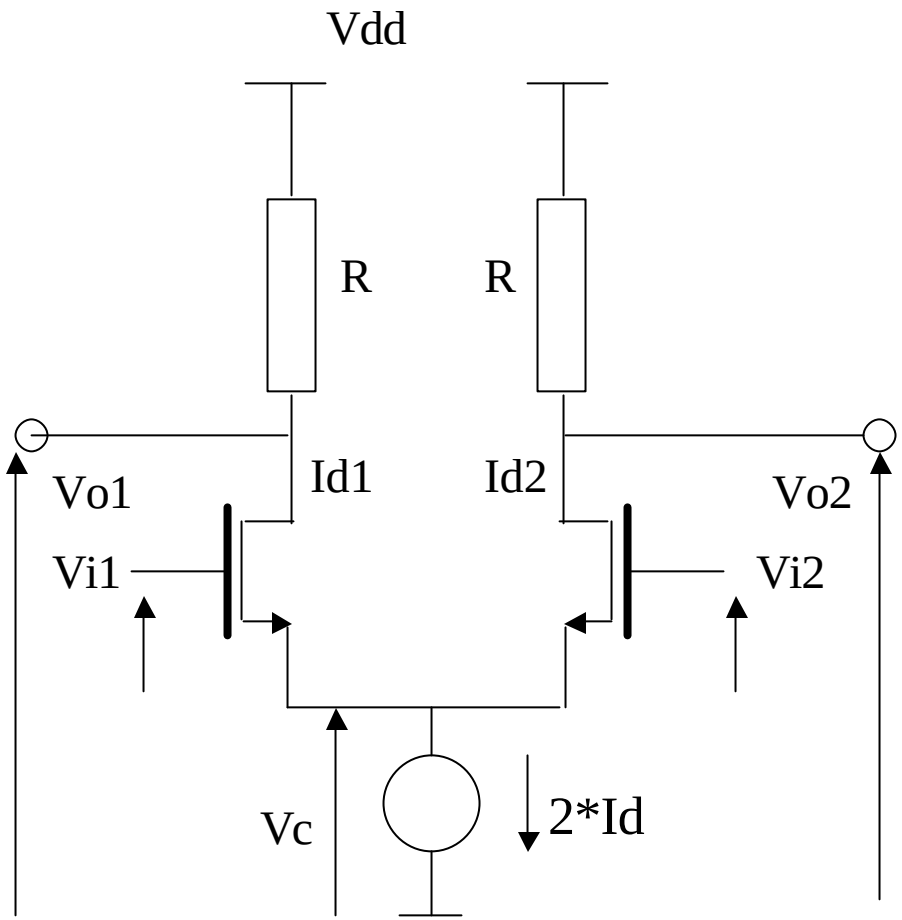
• Output DC is related to input DC levels (no Common Mode Rejection)

5- Differential Amplifier

Because of the weaknesses of the single-ended structure (common-mode and power supply sensitivity), the differential amplifier is usually a preferred structure



5 - Differential Amplifier



Formulate :

$$Vi1 = Vid/2 + Vcm$$

$$Vi2 = -Vid/2 + Vcm$$

Vid is the differential signal at input
Vcm the input signal common mode
Vc the voltage to transistor source

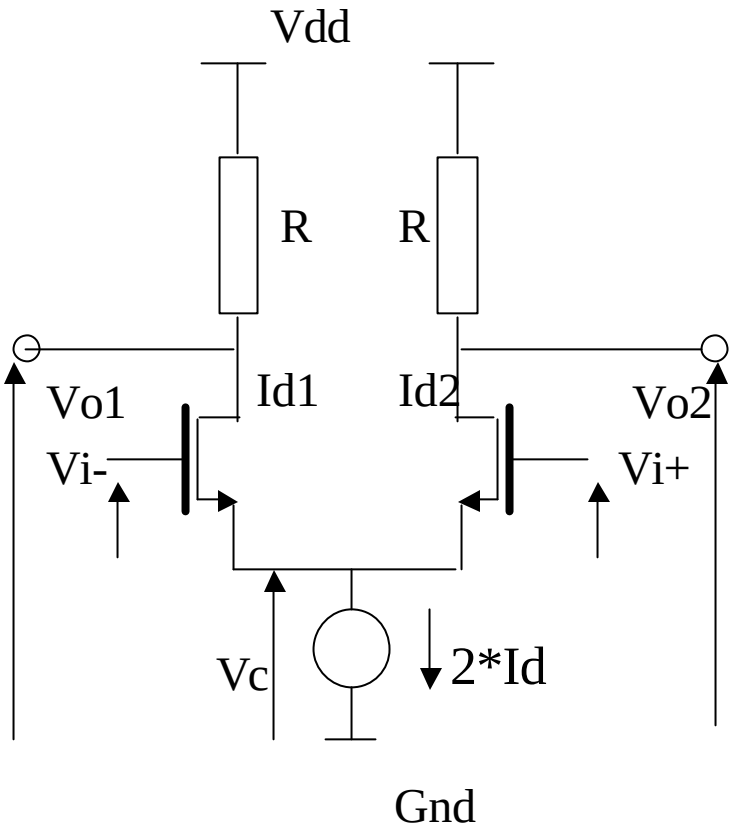
From MOS transistor equations :

$$Id1 = k0.\frac{W}{L}.(Vid/2 + Vcm - Vc - Vt)^2$$

$$Id2 = k0.\frac{W}{L}.(-Vid/2 + Vcm - Vc - Vt)^2$$

5 - Differential Amplifier

Vid is the differential signal at input
Vcm the input signal common mode
Vc the voltage to transistor source



Differential Gain :

Small signal Formulation, diff. Input variation :

$$id1 = 2.k0.\frac{W}{L}.(Vcm - Vc - Vt).Vid/2$$

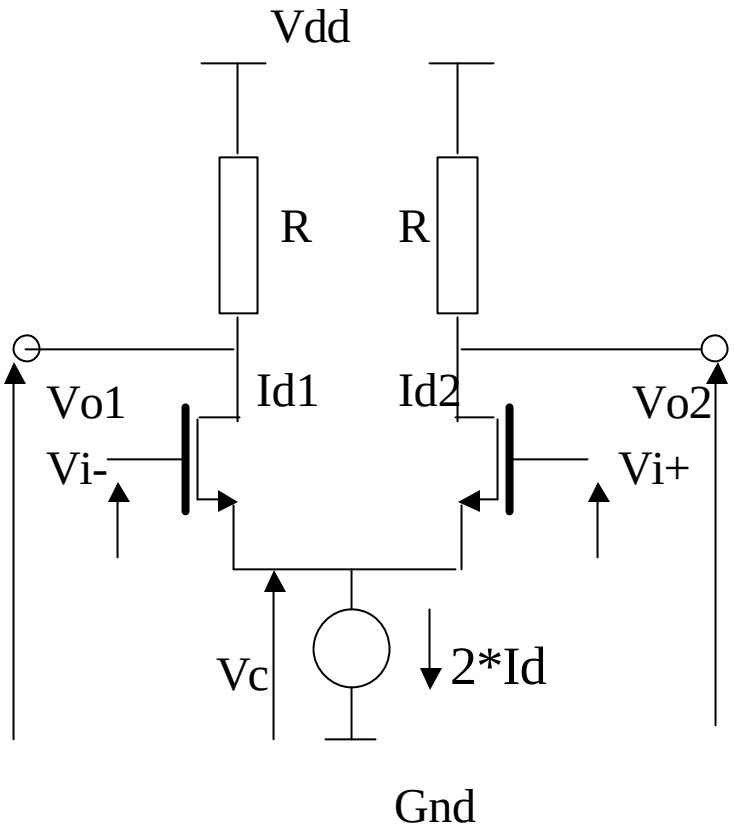
$$id2 = -2.k0.\frac{W}{L}.(Vcm - Vc - Vt).Vid/2$$

$$? Vo = Vo2 - Vo1 = R(id2 - id1)$$

$$? Vo = 2.R.k0.\frac{W}{L}.(Vcm - Vc - Vt).Vid$$

5 - Differential Amplifier

Vid is the differential signal at input
Vcm the input signal common mode
Vc the voltage to transistor source



$$(Vcm - Vc - Vt) = \sqrt{\frac{Id}{ko.W/L}}$$

$$? Vo = 2.R.\sqrt{k0.\frac{W}{L}.Id.Vid}$$

$$gm = 2.\sqrt{k0.\frac{W}{L}.Id}$$

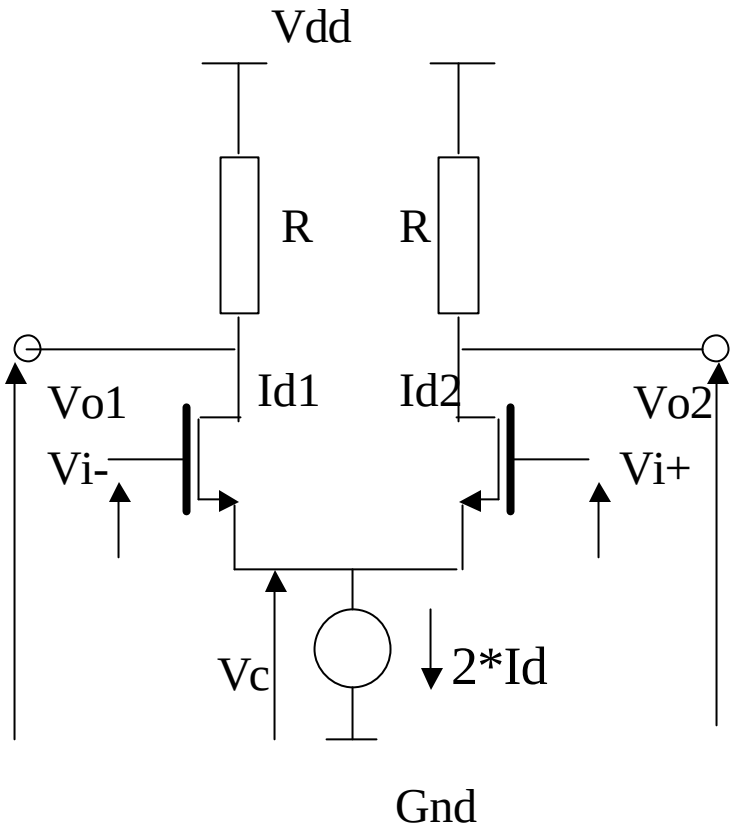
Is the input transistors transconductance

We end up with the differential gain expressed as :

$$G = R.gm$$

5 - Differential Amplifier

Vid is the differential signal at input
Vcm the input signal common mode
Vc the voltage to transistor source



Common Mode Gain :

Small signal Formulation, Common Mode Input variation :

$$id1 = 2.k0.\frac{W}{L}.(Vcm - Vc - Vt).(v_{cm} - v_c)$$

$$id2 = 2.k0.\frac{W}{L}.(Vcm - Vc - Vt).(v_{cm} - v_c)$$

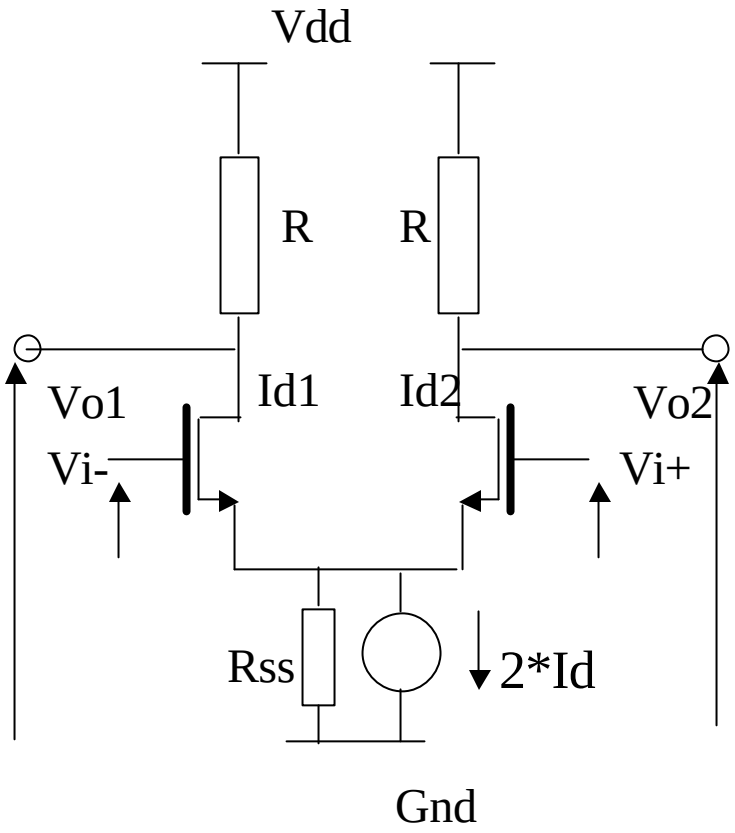
If the tail current source is perfect (very high Z) :

$$id1 + id2 = 0 \Longrightarrow id1 = 0 \text{ and } id2 = 0$$

Vo outputs are insensitive to common mode input

5 - Differential Amplifier

Vid is the differential signal at input
Vcm the input signal common mode
Vc the voltage to transistor source



Common Mode Gain :

If the tail current source has impedance Rss

$$\frac{v_o}{v_{cm}} = \frac{R.gm}{1+2gmRss}$$

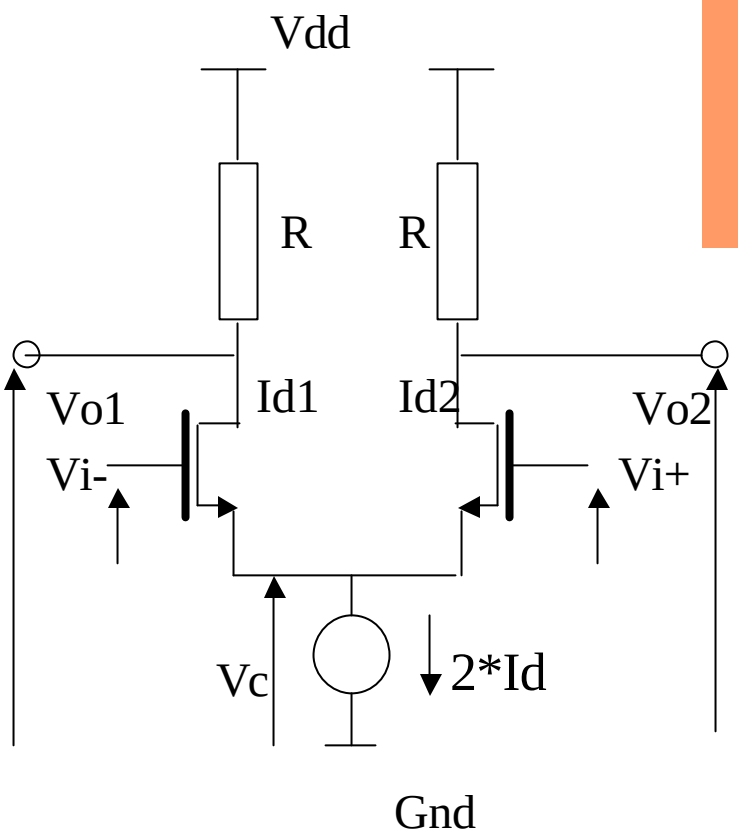
This is the common mode gain, which is much less than the differential gain, approx. by the factor R/(2Rss).

The ratio of the differential gain to the common mode gain, is called the Common Mode Rejection Ratio (CMRR). In our case :

$$CMRR \cong 2gmRss$$

(CMRR easily reaches 1000 (60db))

5 - Differential Amplifier



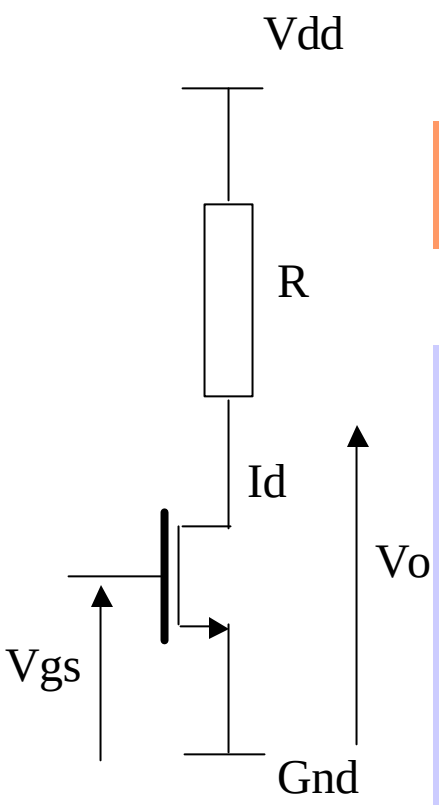
By similar reasoning, it can be shown that the differential structure can provide :

- High Common Mode Rejection
- High Power Supply Rejection

The other features are :

- Differential gain formulation as for single-ended
- Constant power consumption

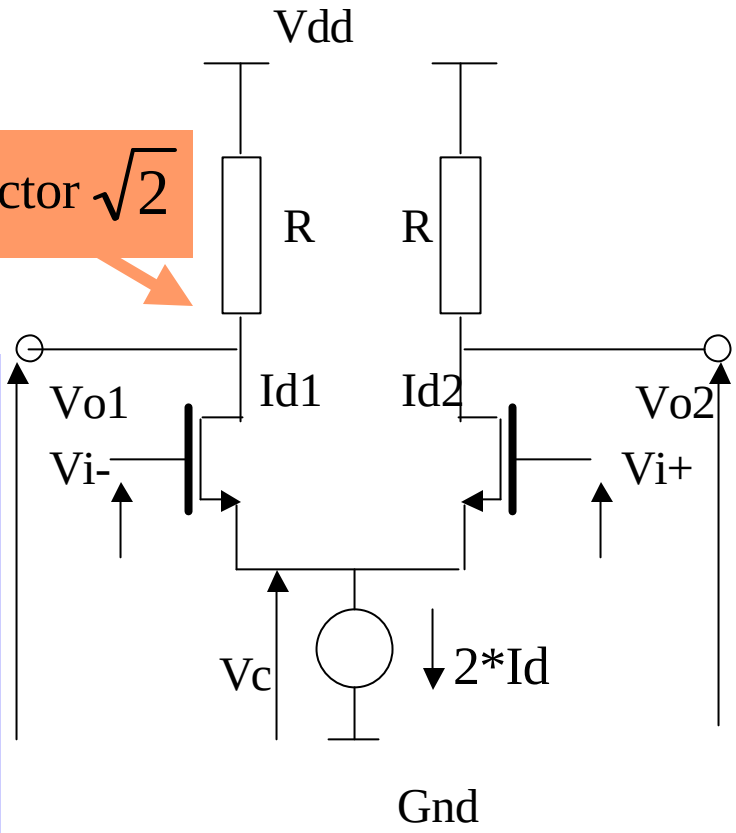
5 - Differential Amplifier



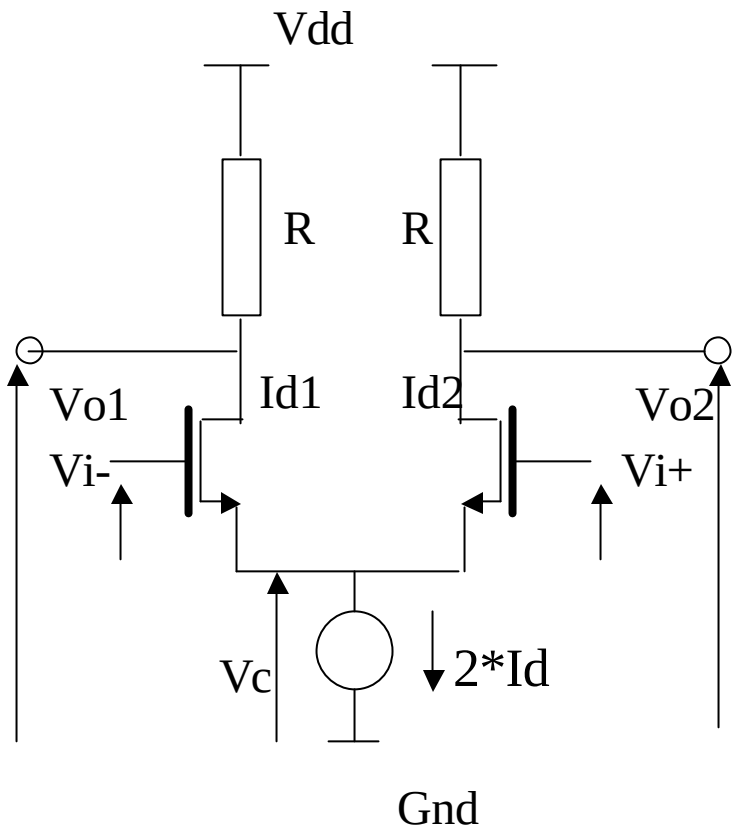
Drawback: Noise increase by factor $\sqrt{2}$

When noise level is critical, as in case of small detector signals, the single-ended option is the preferred choice.

It is at the cost of higher sensitivity to common-mode and power supply noise.



5 - Differential Amplifier



• Limited “open loop” gain

Typical Example :

$$G = \mathrm{R.gm}$$

$$\mathrm{gm} = 10^{-3}$$

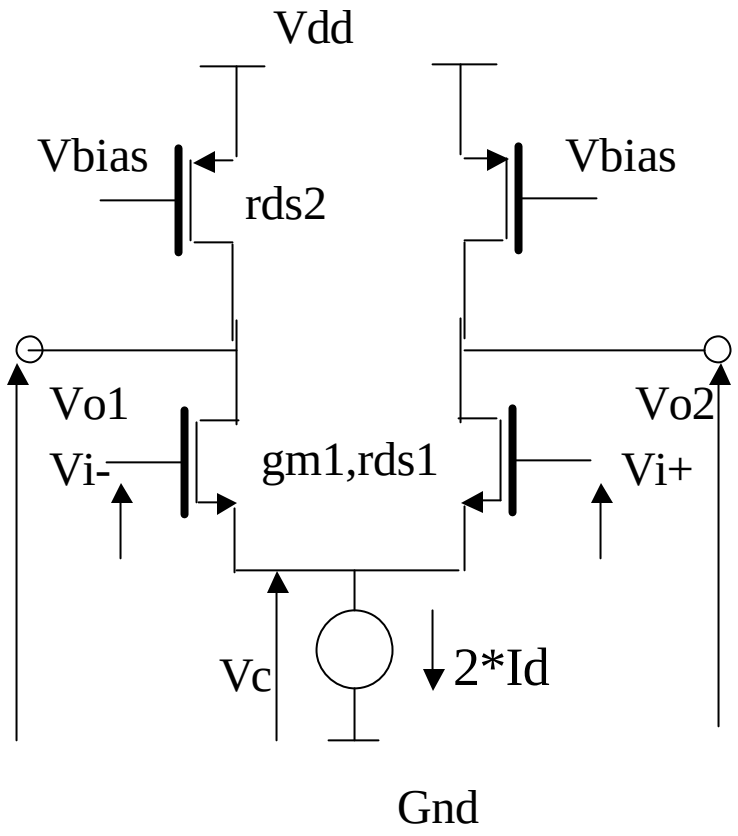
$$\mathrm{R} = 10\mathrm{K}$$

$$G = 10!$$

• Open-loop Gain, DC point and Output Impedance are correlated by R

• “one-pole” system assumes stability

6 - Active Load ; OTA



- The resistive load “R” is replaced by an active device (transistor) of transconductance gm2

$$G = gm1.rds$$

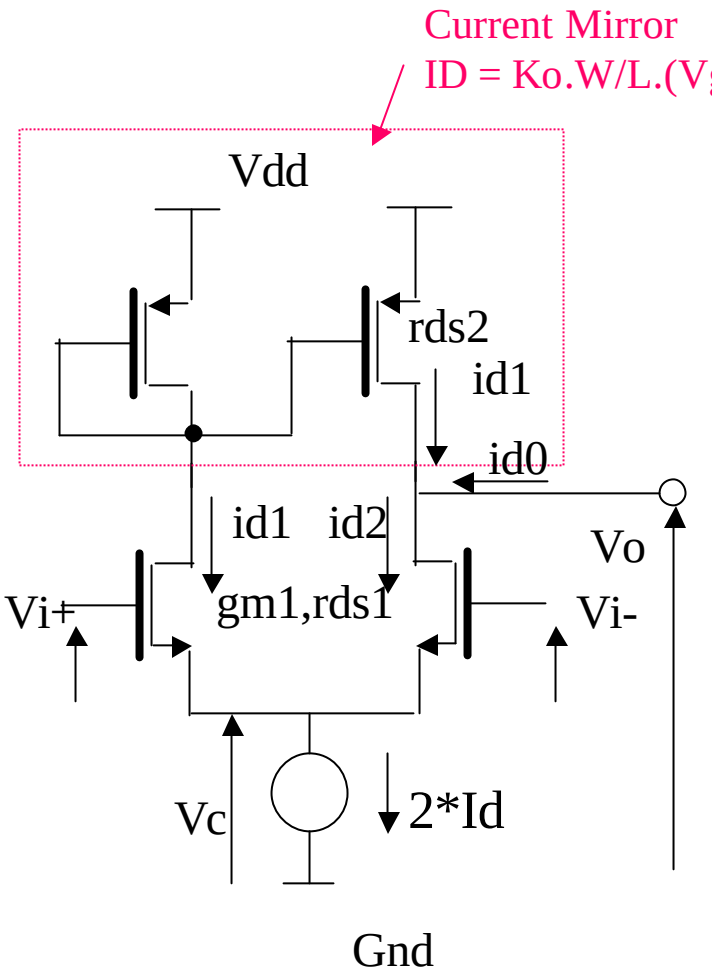
$$rds = rds1//rds2$$

- The amplifier is only made of complementary transistors (Pmos, Nmos).

- “MOS-only” circuit makes it compatible with most standard digital process.

$$G \geq 100$$

6 - Active Load ; OTA



In this configuration, the current in the output branch (ido) is the difference between the two currents variations in the two input devices :

$$id1 = gm1.(vi+)$$

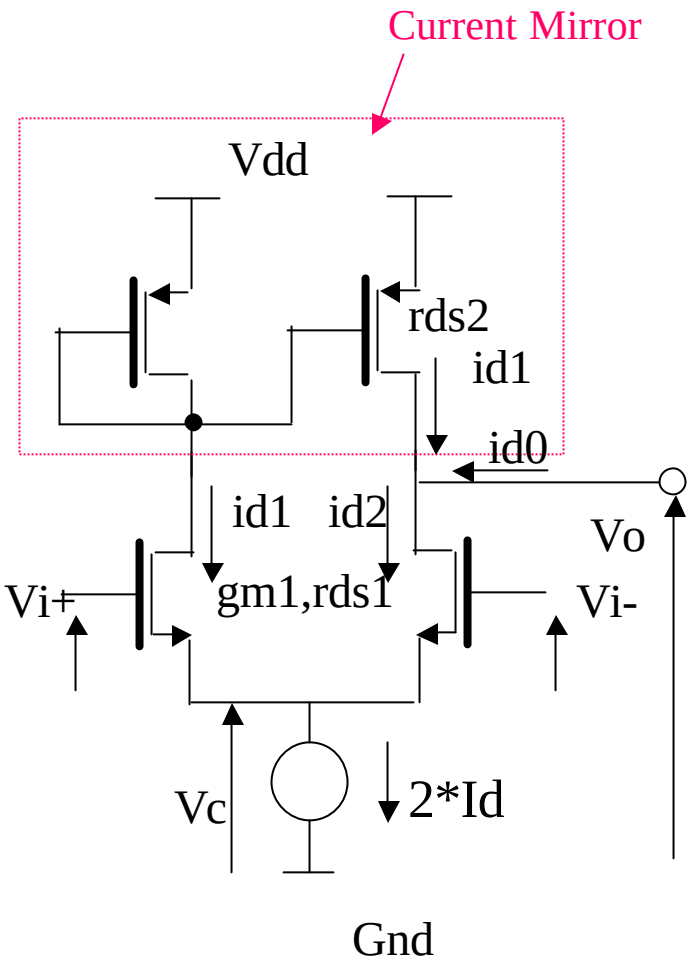
$$id2 = gm1.(vi-)$$

$$ido = gm1.(\Delta vi)$$ (Δvi being the differential input voltage)

Thus the output voltage variation vo is given by

$$vo = Rout.ido = Rout.gm1.\Delta vi$$

6 - Active Load ; OTA

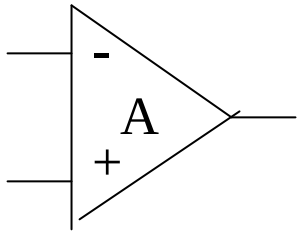


This amplifier configuration is the typical circuit of amplification stages in CMOS technology

• It provides differential inputs to single-ended output

• It has high “DC” gain (opamp) as it is shown in next transparencies

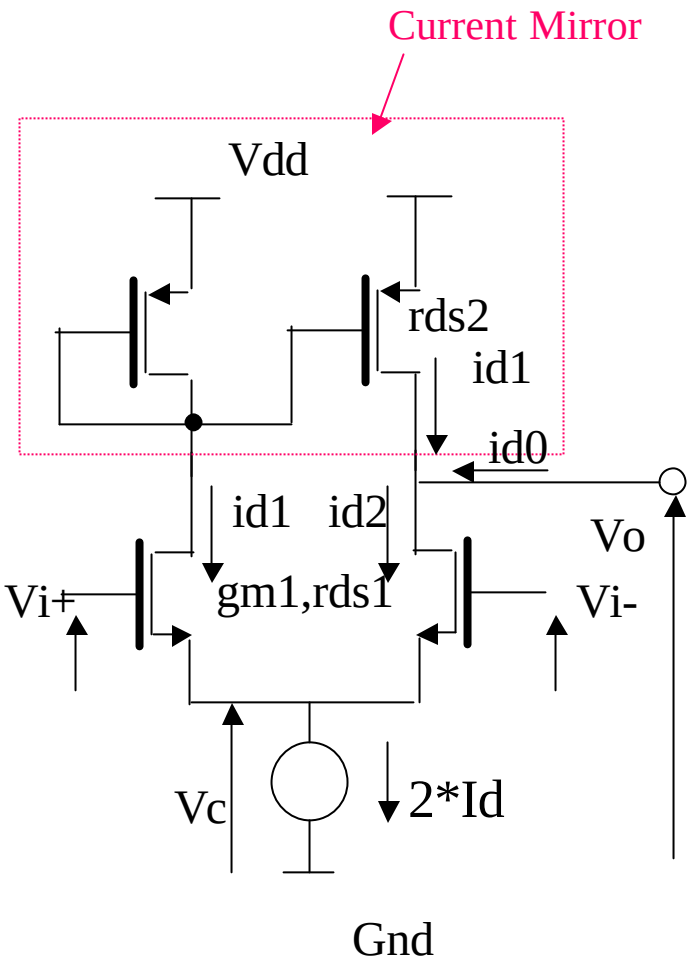
• “one-pole” system (stable)



$$G = rout.gm1$$

What is rout ?

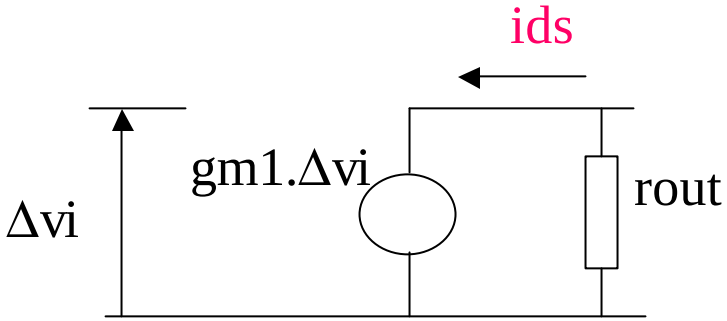
6 - Active Load ; OTA



rout calculation

The output impedance is the equivalent impedance seen from the output node, i.e. :

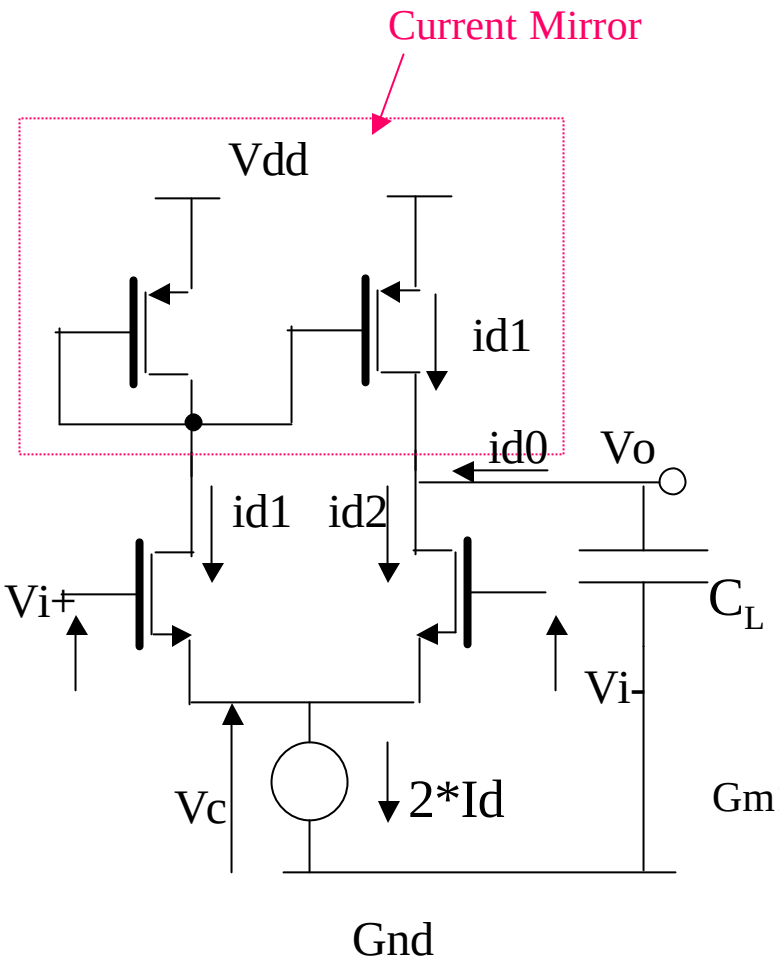
$$rds1 // rds2 = rout$$

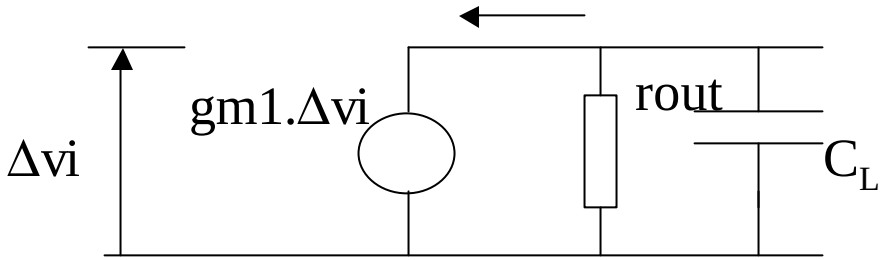


$$G = rout.gm1$$

The output impedance is usually high (50K to 500K), thus one-stage gain is high (gm=1mS, rout= 500K -→ G=500 !)

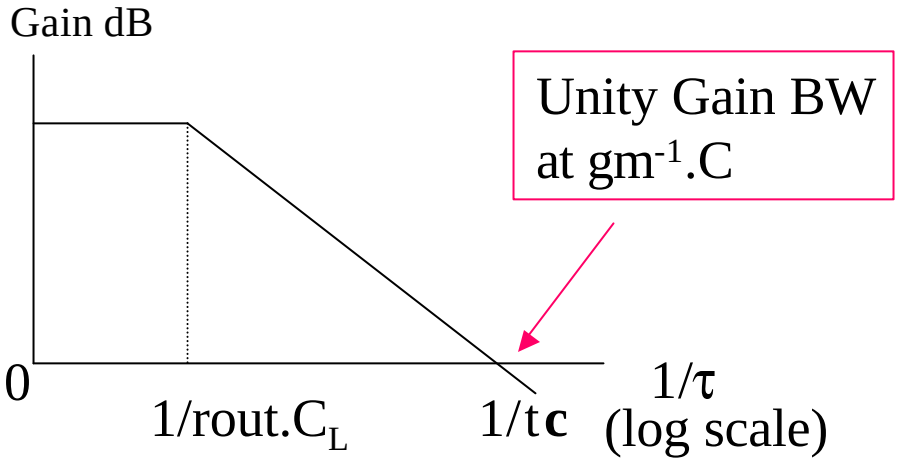
6 - Active Load ; OTA



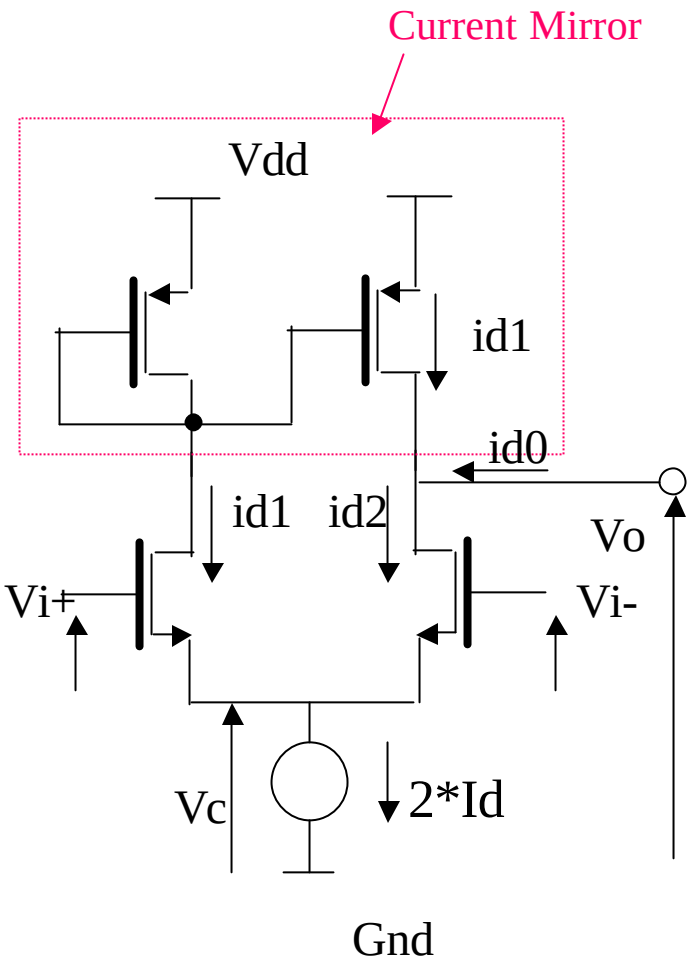


$$G_{DC} = \text{rout.gm1}$$

This amplifier behaves as an opamp.
Large gm gives high DC gain.
Main pole is fixed by the output (rout.C_L) time constant.



6 - Active Load ; OTA



Drawback of this circuit : its limited open-loop DC gain G . If used with a feedback gain β, the output impedance is given as :

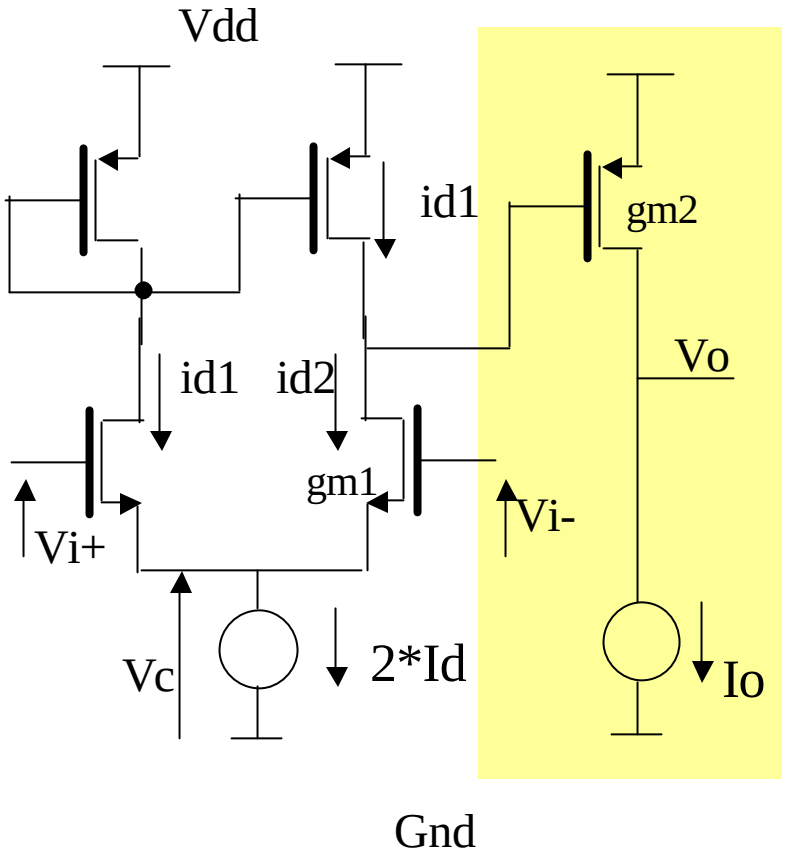
$$Zout \approx rout_{OL} \cdot \frac{1}{b \cdot G}$$

N.A. : G=500, β=0.1 -→ Zout = 10Kohms

It is not suitable for resistive load (50 to 1Kohms range).

It fits well for application with pure capacitive load, where low output impedance or large current are not required (many examples in switched capacitor circuits, SC filters).

7 - Two Stage Differential Amplifier



Add single-ended second stage

2nd stage can draw a large current (gm2 large)

$$G_{DC} = G1.G2$$

$$G_1 = gm1.rout1$$

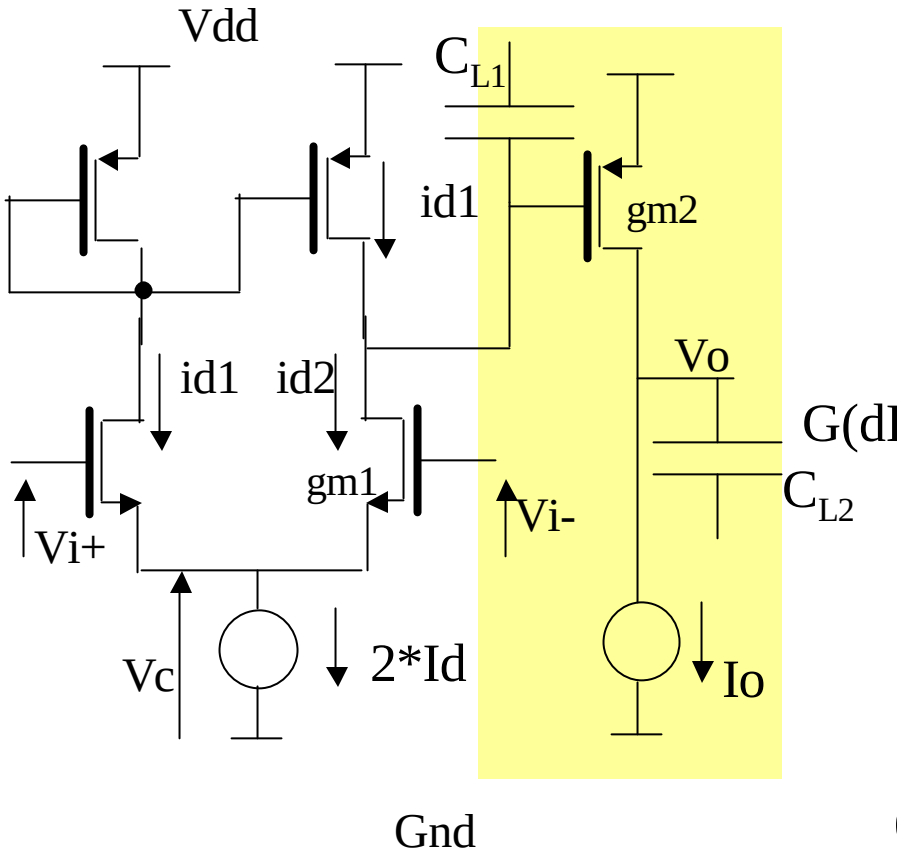
$$G_2 = gm2.rout2$$

N.A : gm1 = 0.5mS gm2 = 3mS
rout1 = 1M rout2= 200K

=➔ G_{DC}=30000 (90 dB)

Output impedance. : G=30000, β=0.1 -➔ Zout = 66 ohms

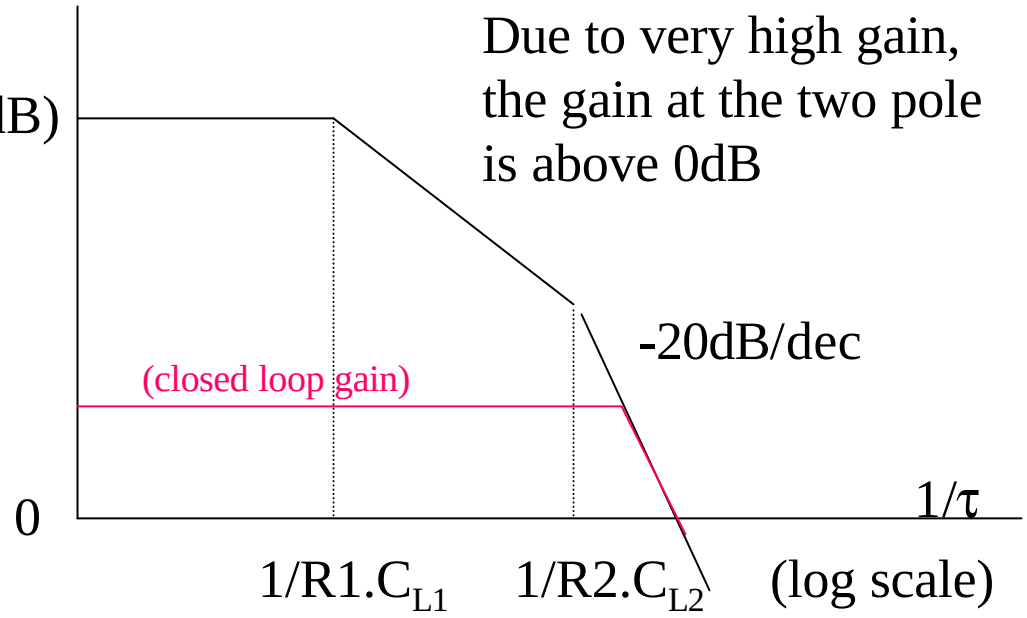
7 - Two Stage Differential Amplifier



There are two poles

First pole : rout1.C_{L1}

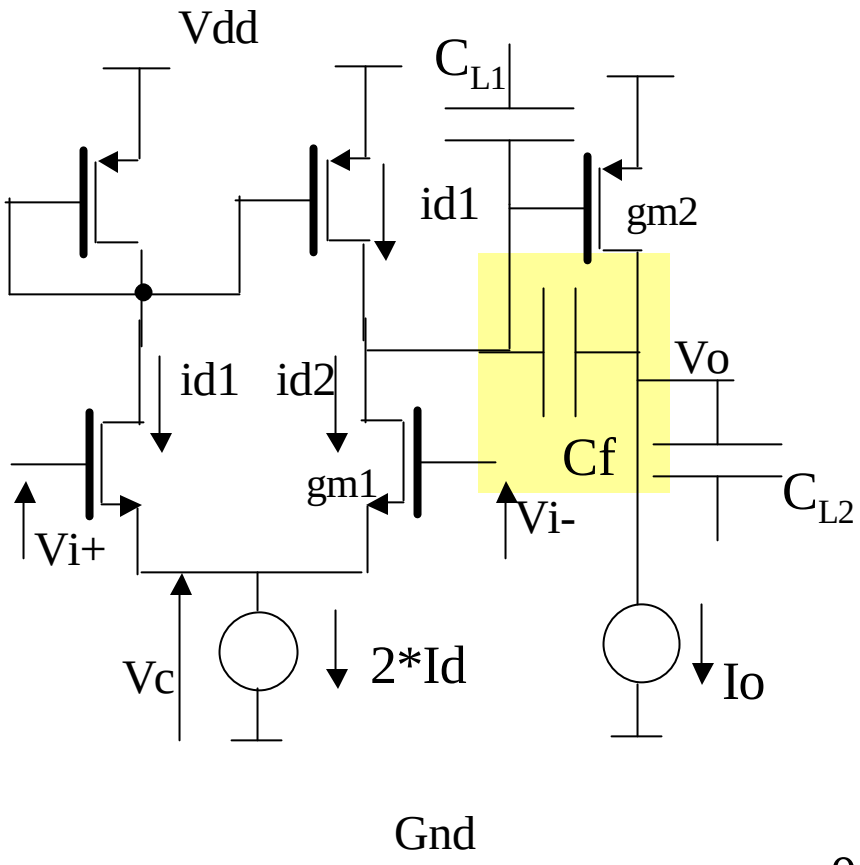
Second pole : rout2. C_{L2}



INSTABILITY

7 - Two Stage Differential Amplifier

Miller Capacitance Cf

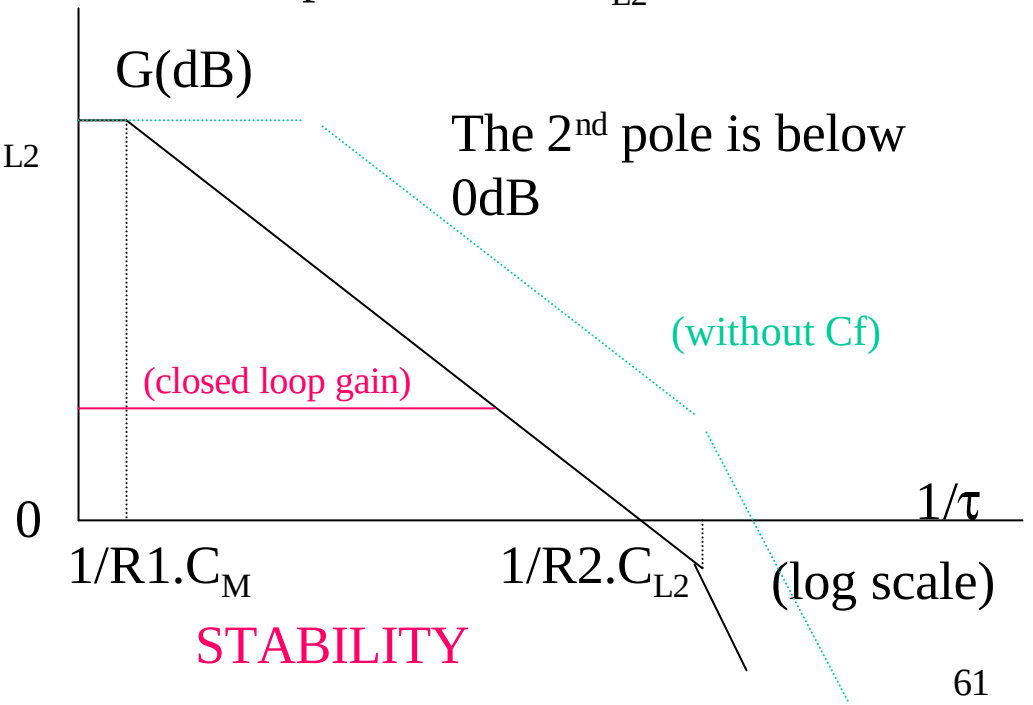


The Cf capacitance is seen by first stage as load of value (Miller effect)

$$C_M \approx gm2.rout2.Cf$$

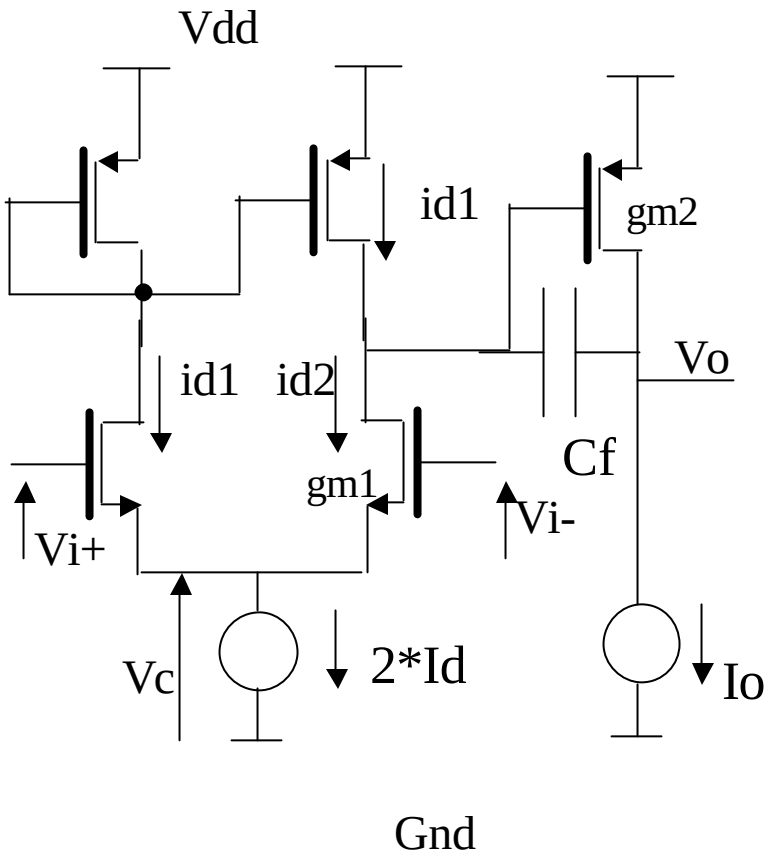
First pole : $rout1.C_M$

Second pole : $rout2.\ C_{L2}$



STABILITY

7 - Two Stage Differential Amplifier



This circuit has the characteristics to behave as a “good” operational amplifier

High Input Impedance (Capacitive only)

High DC Gain (70-90dB)

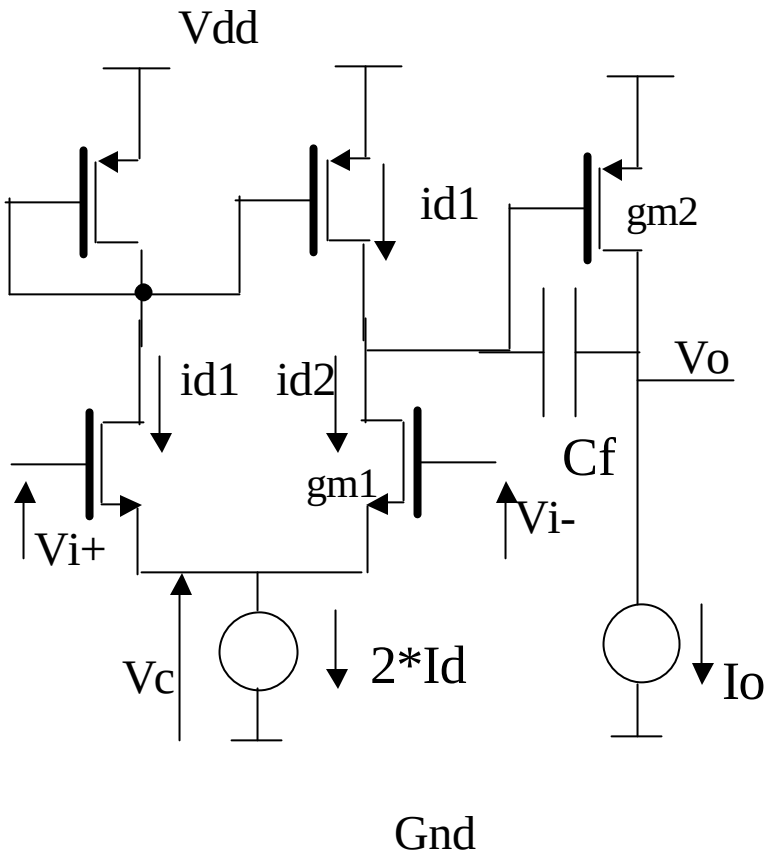
Low output impedance

N.A. : G=30000, β=0.1 -→ Zout = 66 ohms

Widely used circuit. Lot of variations exist (improved output stage, Gain enhancement etc …)

Stability should always be considered carefully (also depends on feedback and load)

7 - Two Stage Differential Amplifier

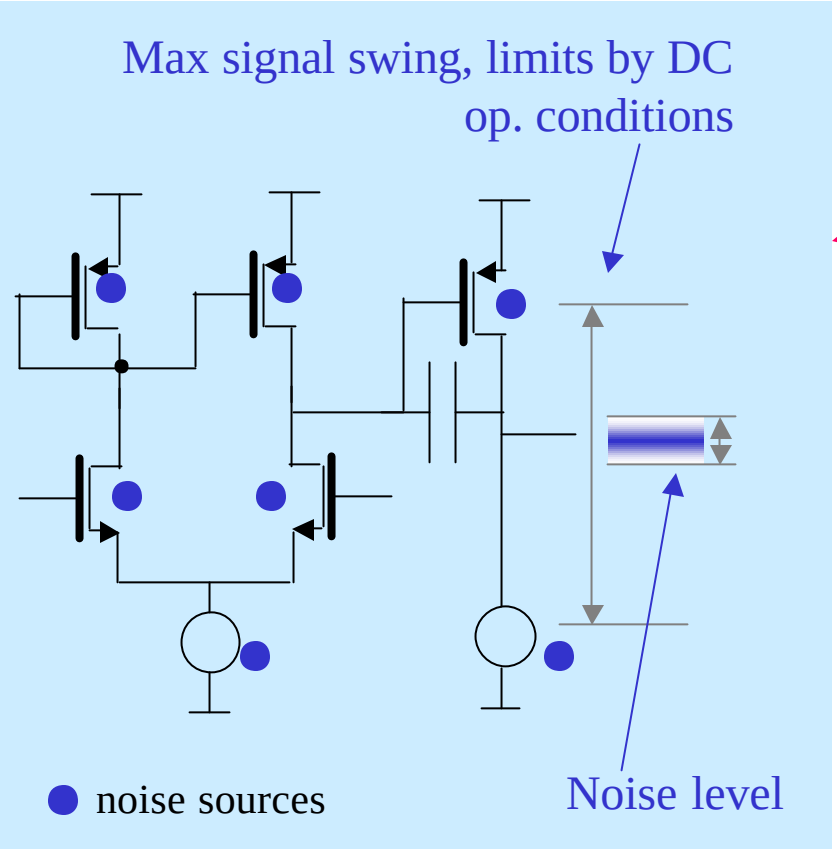


In the preceding discussion we considered only one (main) aspect of the amplifier design (gain and stability)

We did not considered other parameters which have equally large influence on the amplifier design aspects :

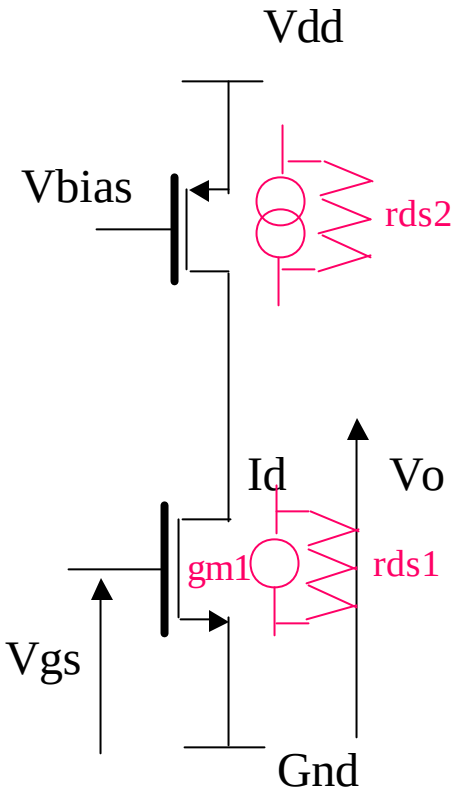
- DC operating point
- Noise figure & dynamic range (S/N ratio)
- Mismatch & Offsets
- Slew rate, large signal behavior
- Power budget

7 - Two Stage Differential Amplifier



- DC operating point : The condition in which each transistor is biased to satisfy its “small signal model”
- Noise figure & dynamic range (S/N ratio) see figure
- Mismatch & Offsets : how technological or geometrical discrepancies between two identical components affect DC or AC characteristics
- Slew rate, large signal behavior : absolute limits given by DC conditions
- Power budget : increasing speed (BW) usually means increasing current (gm ~ funct(I))

8 - Other amplifier circuits

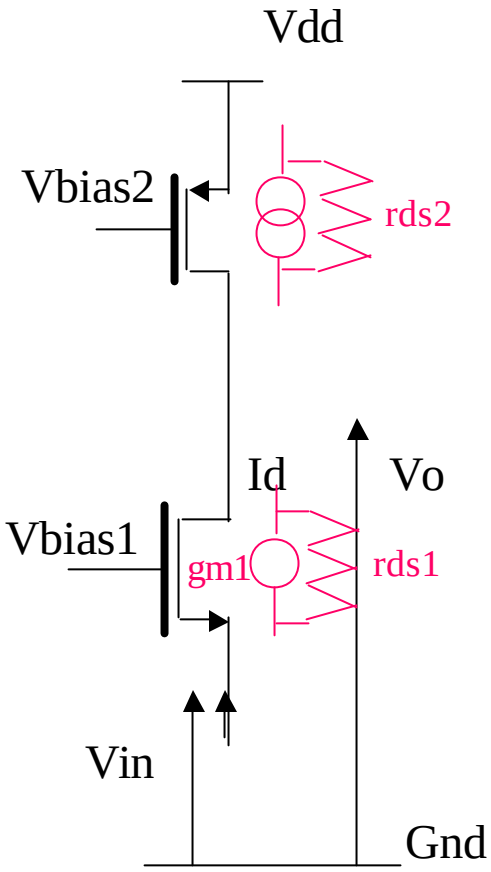


Common Source

- High Input Impedance $Rin = \infty$
- Voltage gain $G_{DC} = rout.gm1$
- High ouput impedance $rds1//rds2 = rout$

8 - Other amplifier circuits

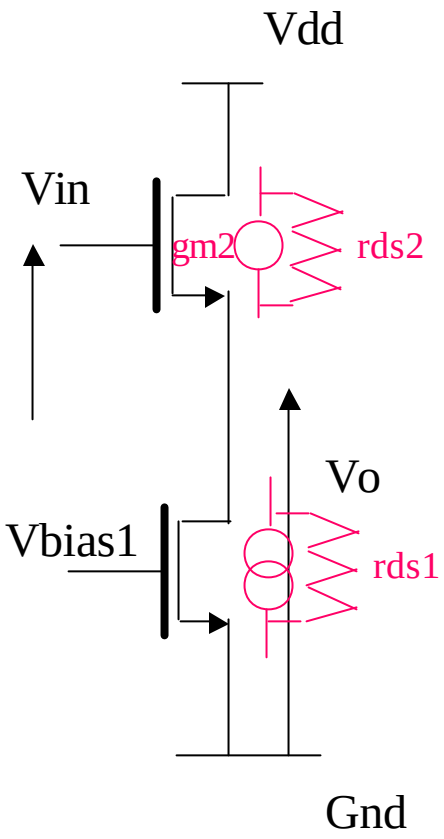
Common Gate



- Low Input Impedance $Rin = (n.gm1)^{-1}$
- Voltage gain $G_{DC} = rout.n.gm1$
- Unity current gain
- High ouput impedance $rds1//rds2 = rout$

(n is a factor specific to the technology, between 1 and 1.5)

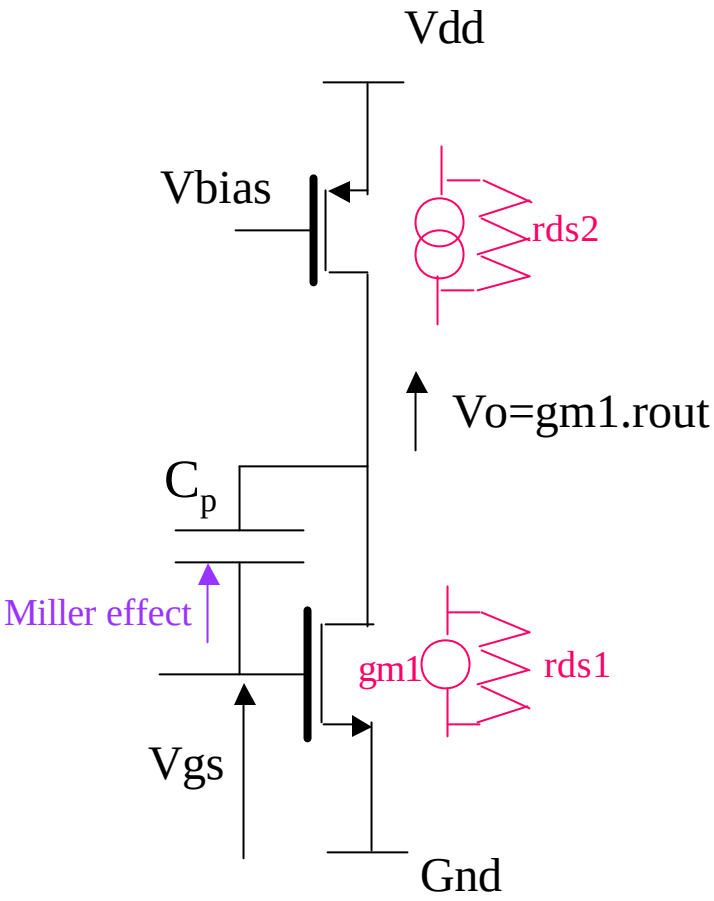
8 - Other amplifier circuits



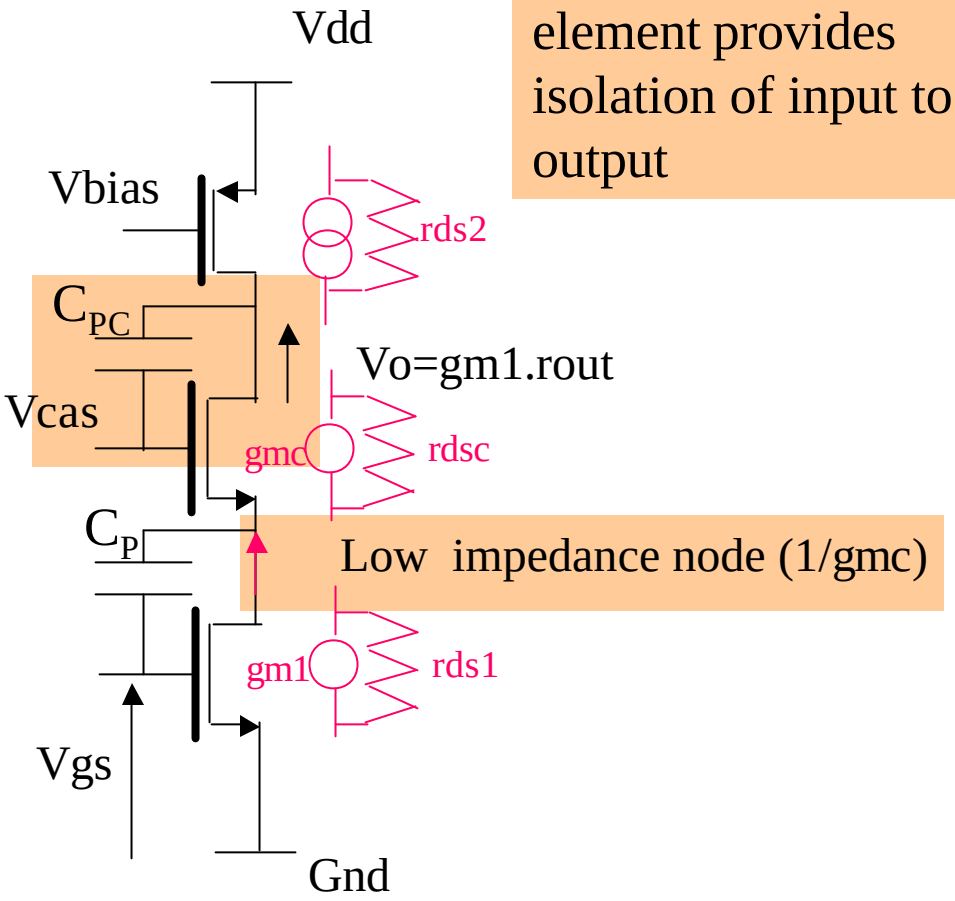
Common Drain
(Source Follower)

- High Input Impedance $Rin = \infty$
- (close to) Unity Voltage gain
- "low" output impedance $rout \approx 1/gm2$

9 – Cascode circuit



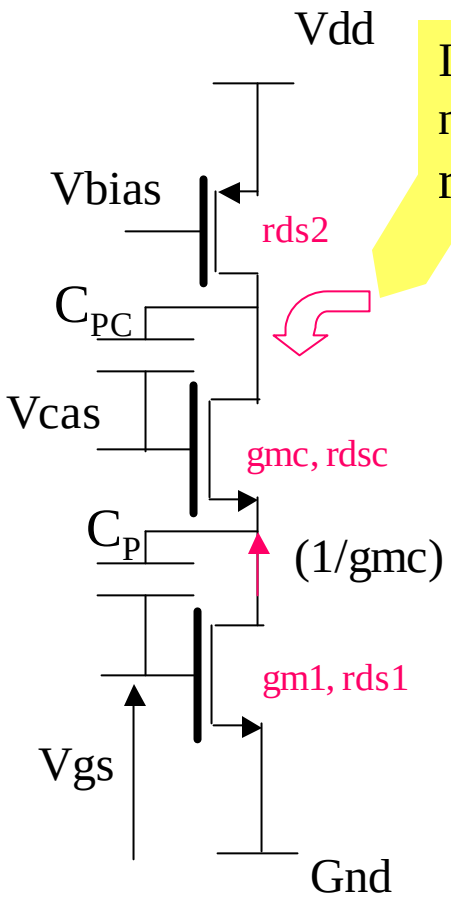
Single ended, without cascode



Single ended, with cascode

The cascode element provides isolation of input to output

9 – Cascode circuit



Impedance seen from output node toward Gnd is : rds1.(1+gmc.rdsc)

Voltage gain is given as :

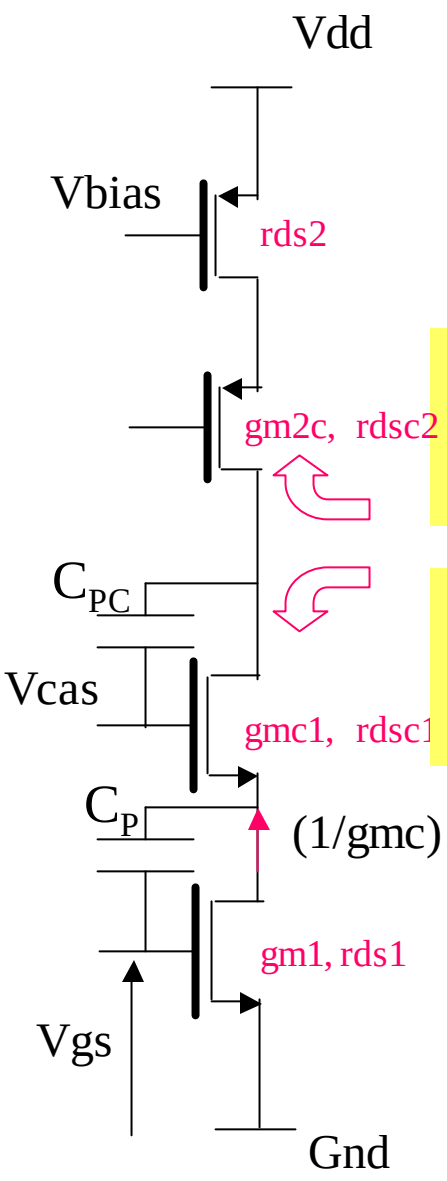
G=gm1.rout

With rout=rds2//rds1.(1+gmc.rdsc)

As gmc.rdsc is large (50 to 100)

$$G_{DC} \approx gm1.rds2$$

9 – Cascode circuit



Impedance seen from output node toward Vdd is :
rds2.(1+gmc2.rdsc2)

Impedance seen from output node toward Gnd is :
rds1.(1+gmc1.rdsc1)

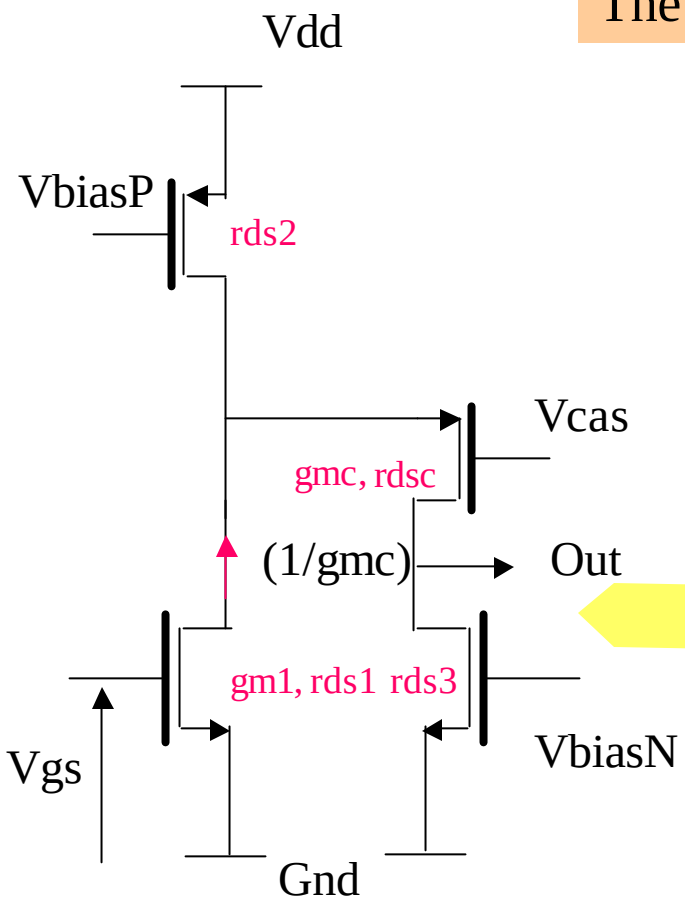
$$G_{DC} = gm1.rout$$

With rout = rds2(1+gmc2.rdsc2) //rds1.(1+gmc1.rdsc1)

DC gain can be very large in one stage (>60db)

9 – Cascode circuit

The folded cascode circuit

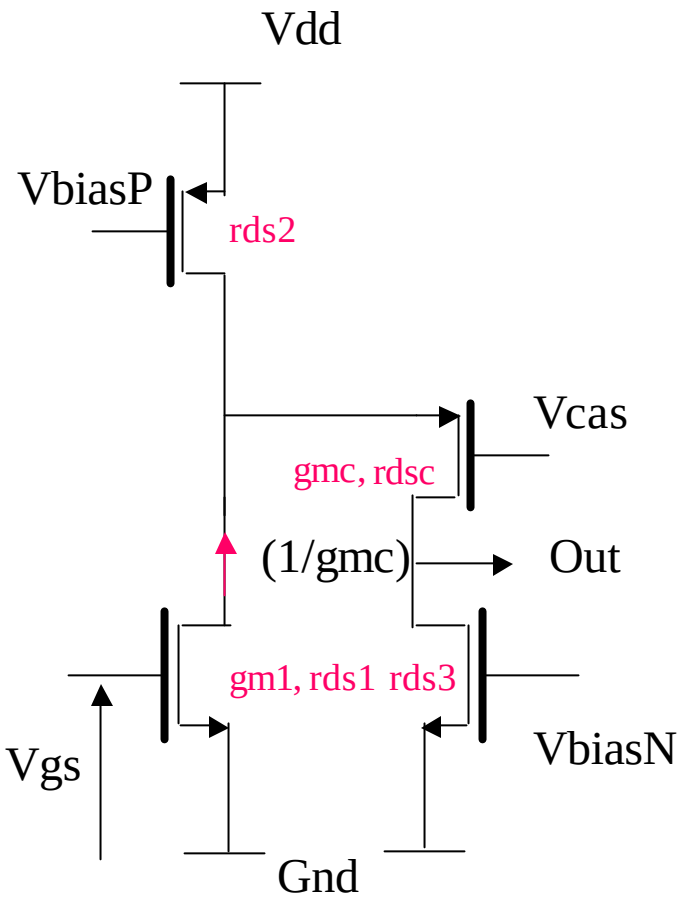


$G_{DC} \approx gm1.rout$

rout=rds3//rds1.(1+gmc.rdsc)

Impedance seen from output node is rds3//rds1.(1+gmc.rdsc)

9 – Cascode circuit



The folded cascode circuit

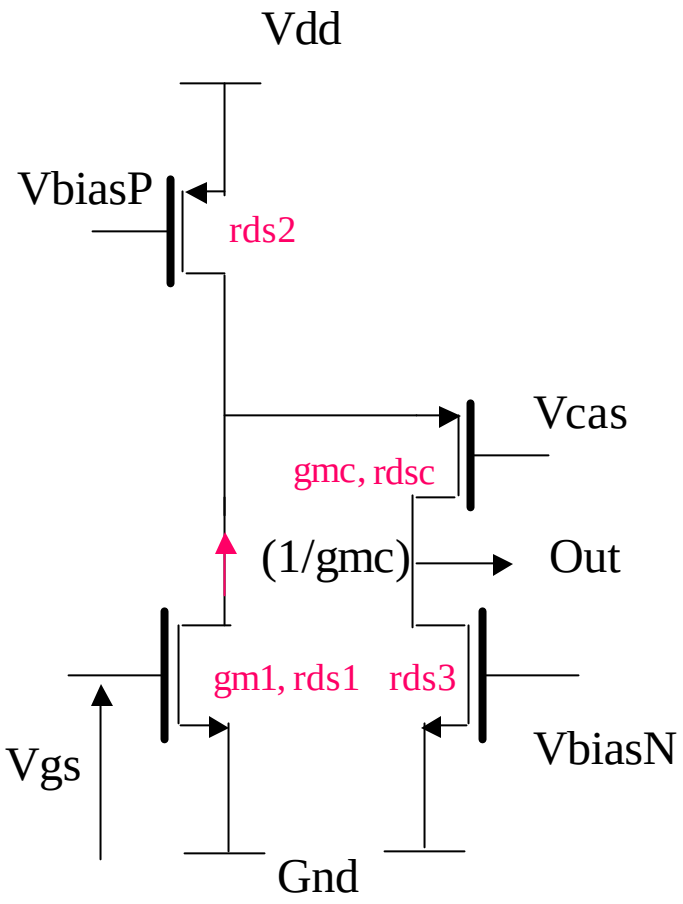
This circuit arrangement has virtually many advantages :

- High DC gain
- One pole system (2nd pole is at very high frequencies). Stability improves if capacitive load is increasing.
- DC operating points at input and outputs are similar

One drawback :

- Limited output voltage swing

9 – Cascode circuit

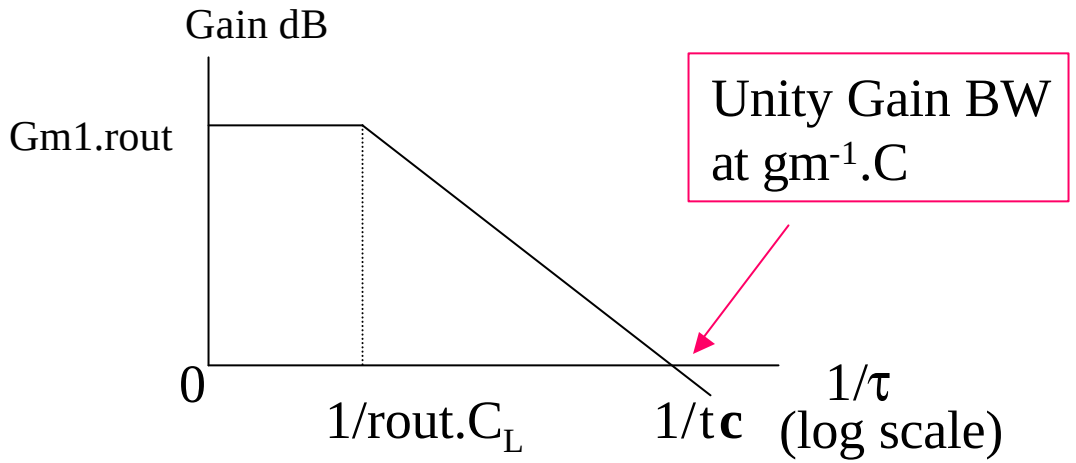


The folded cascode circuit

This circuit is the basic one used for charge preamplifier design in detector readout

$G_{DC} \approx gm1.rout$

rout=rds3//rds1.(1+gmc.rdsc)



End of First Part

What we have presented:

The Bipolar device as an amplifying component

Basic amplifiers schemas (Bipolar or MOS components)

General purpose two stage amplifier

Differential vs. Single-Ended

What we will do in 2nd part:

Look at two detector signal preamplifier configurations (charge sensitive amplifier and transimpedance amplifier)